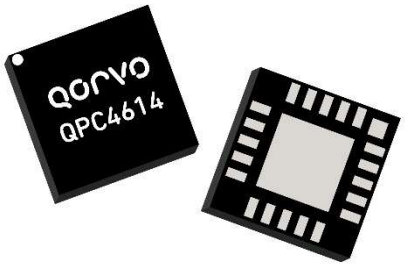
QPC4614

75Ω 5 –2000MHz Digital Step Attenuator

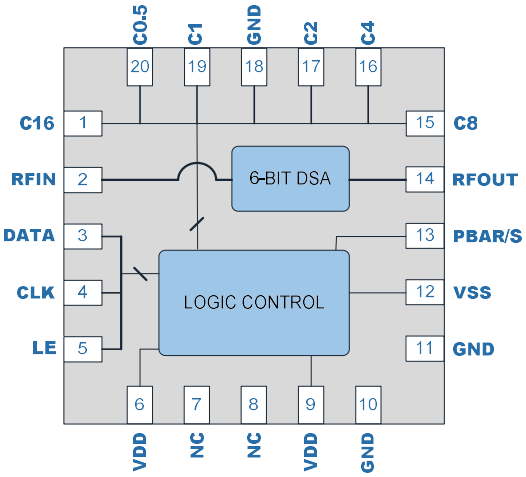
Product Overview

The QPC4614 is a 75Ω 6-bit digital step attenuator (DSA) that features high linearity over the entire 31.5 dB gain control range in 0.5 dB steps and has a low insertion loss of 1.2dB at 1 GHz. The QPC4614 features three modes of control: serial, latched parallel, and direct parallel programming. Patented circuit architecture provides overshoot-free transient switching performance. QPC4614 is available in a 20-pin 4 x 4mm QFN package.



20 Pin 4 x 4mm QFN Package

Functional Block Diagram



Top View

Key Features

- 6-Bit, 31.5dB Range, 0.5dB Step
- Patented Circuit Architecture
- Frequency Range 5MHz to 2000MHz
- High Linearity, IIP3 69dBm Typical at 850MHz
- Serial and Parallel Control Interface
- RF Pads Have No DC Voltage; Can be DC Grounded Externally
- Option to Turn Off Negative Voltage Generator and Supply V_{SS} Externally
- Power-up Default Setting Is Maximum Attenuation

Applications

- Optical Nodes
- Point-to-Point
- MDU Amplifiers
- Pre-amplifier Attenuation
- Inter-stage Attenuation
- Return Attenuation
- AGC
- Tilt Control

Ordering Information

Part No.	Description
QPC4614SB	Sample bag with 5 pieces
QPC4614SR	7" Reel with 100 pieces
QPC4614TR13	13" Reel with 2500 pieces
QPC4614EVB-01	5 - 2000 MHz PCBA

Absolute Maximum Ratings

Parameter	Rating
Supply Voltage (V_{DD})	-0.5 to +6.0V
Supply Voltage (V_{SS})	-6.0 to +0.5V
All Other DC and Logic Pads (Supply Voltage Must Be Applied Prior to Any Other Pin Voltage)	-0.5 to VDD
Maximum Input Power at 85 °C Case Temperature	+31dBm
Maximum Input Power at 105 °C Case Temperature	+29.5dBm
Storage Temperature Range	-40 to +150°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage, V_{DD}	+2.7	+5.0	+5.5	V
Supply Voltage, V_{SS}	-5.5	-5.0	-4.5	V
Maximum Input Power at 85 °C Case Temperature			28.5	dBm
Maximum Input Power at 105 °C Case Temperature			25.5	dBm
Temperature Range	-40		+105	°C
Junction Temperature			+125	°C

(1) Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

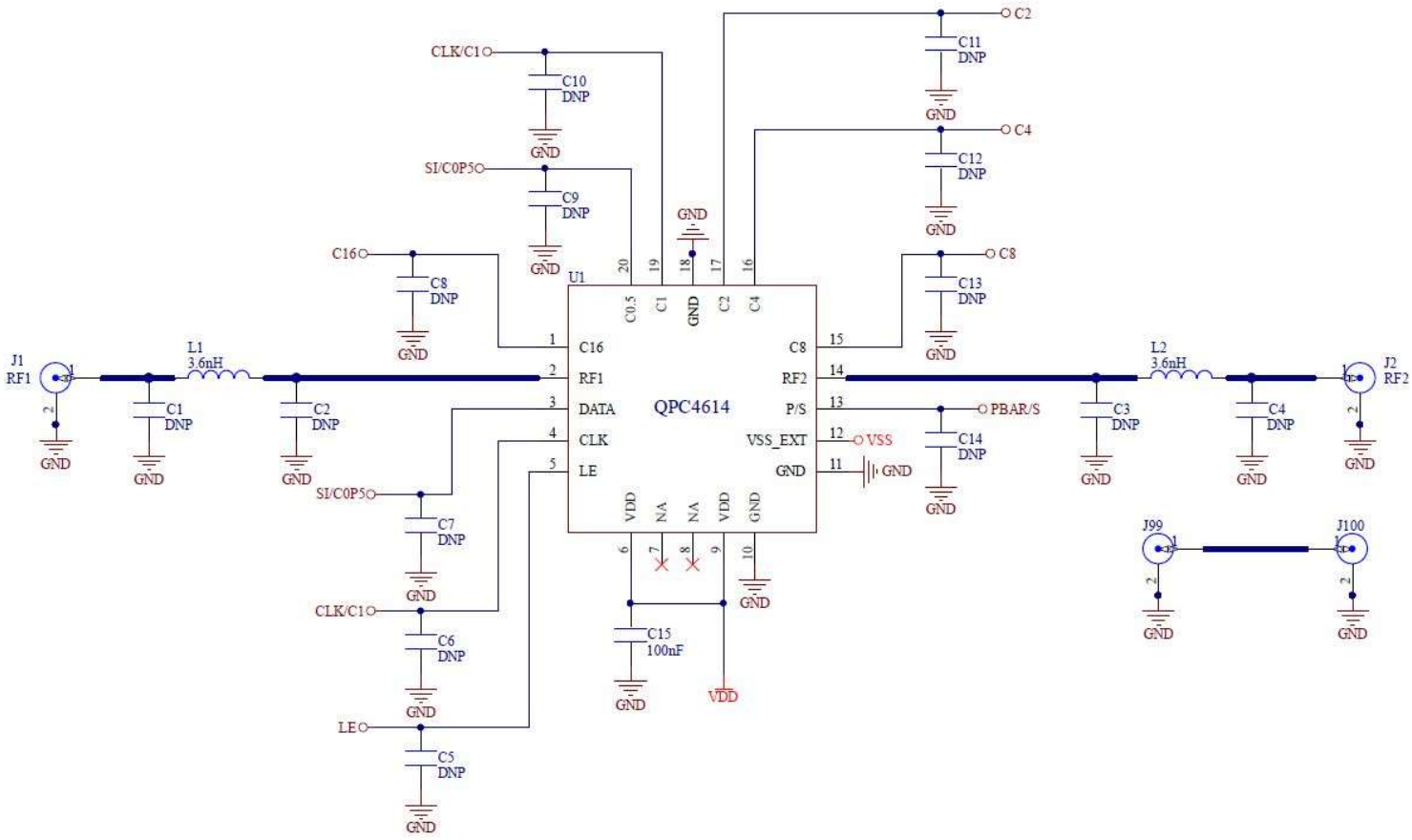
Electrical Specifications

Parameter	Condition (1)	Min	Typ		Max	Unit
Supply Current (I_{DD})	Steady state operation, current draw during attenuation state transitions is higher.		200			µA
Supply Current (I_{SS})	Steady state operation, current draw during attenuation state transitions is higher.		100			µA
Frequency Range		5			2000	MHz
Insertion Loss	1GHz		1.2			
Maximum Attenuation	0.5dB Step Size		31.5			dB
Absolute Attenuation Error			±(0.2 + 4%)			dB
Input IP3(3)	Attenuation Setting:		0dB	31.5dB		dBm
	5MHz		43.5	51.6		
	15MHz		43.8	52.0		
	50MHz		48.0	57.3		
	450MHz		64.3	63.4		
	850MHz		69.5	66.1		
	1900MHz		66.9	65.1		
Input P1dB(2)			35			dBm
Return Loss(4)	1200MHz, all states		16.4dB			dB
Input and Output Impedance			75			Ω
Switching Speed	50% control to 10% / 90% RF		150			nsec
Digital Logic Low					0.63	V
Digital Logic High		1.17				V
Thermal Resistance, θjc	Junction to case		54			°C/W

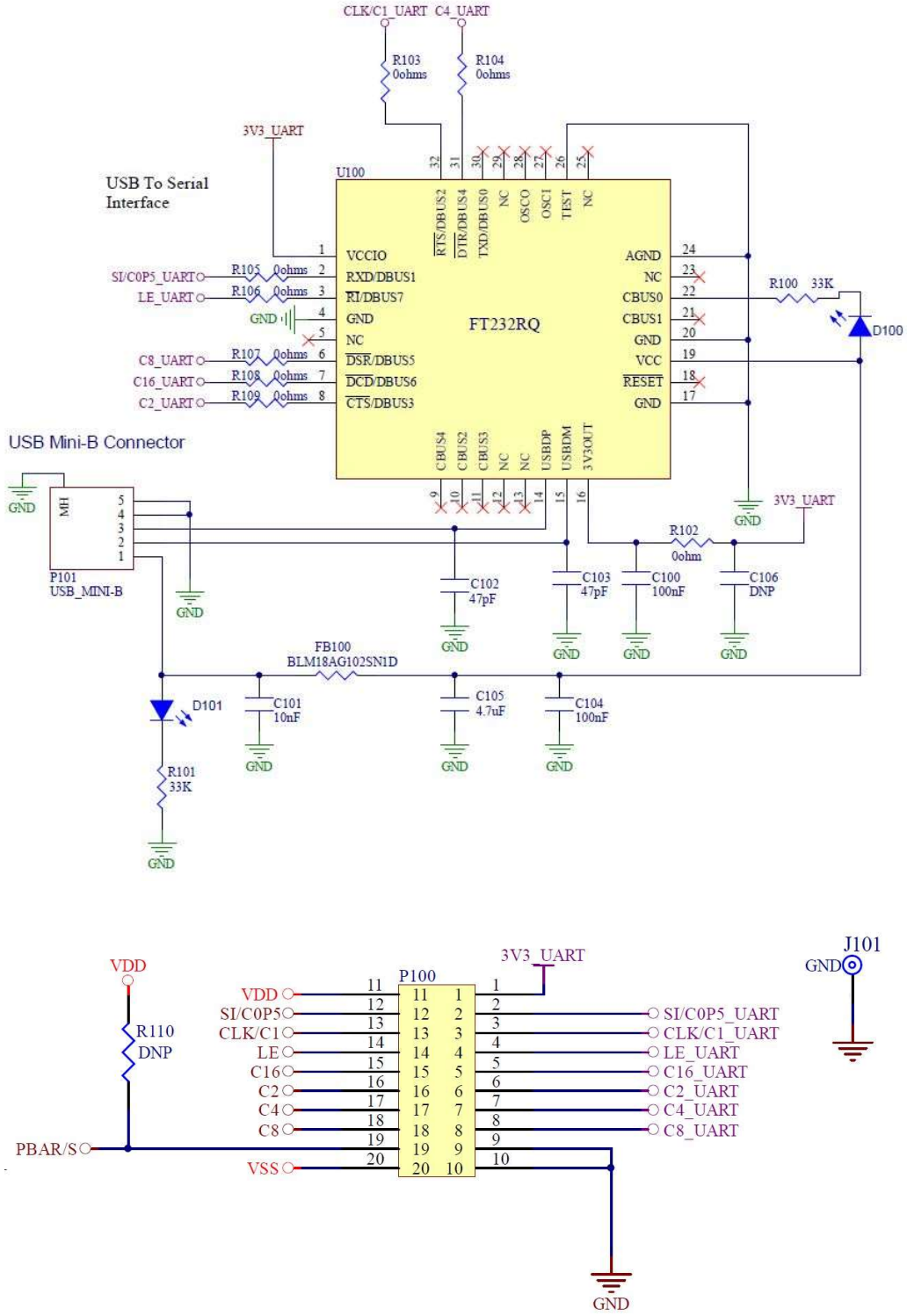
Notes:

1. Typical performance at these conditions: Temp = +25°C, 1000MHz, V_{DD} = +5V, V_{SS} = 0V, 75Ω system.
2. Figure of merit – exceeds maximum input power of device.
3. +12dBm/tone, 25C.
4. Using series-L Match shown in EVB Schematic on pg. 3.

Evaluation Board Schematic; 5 – 2000MHz



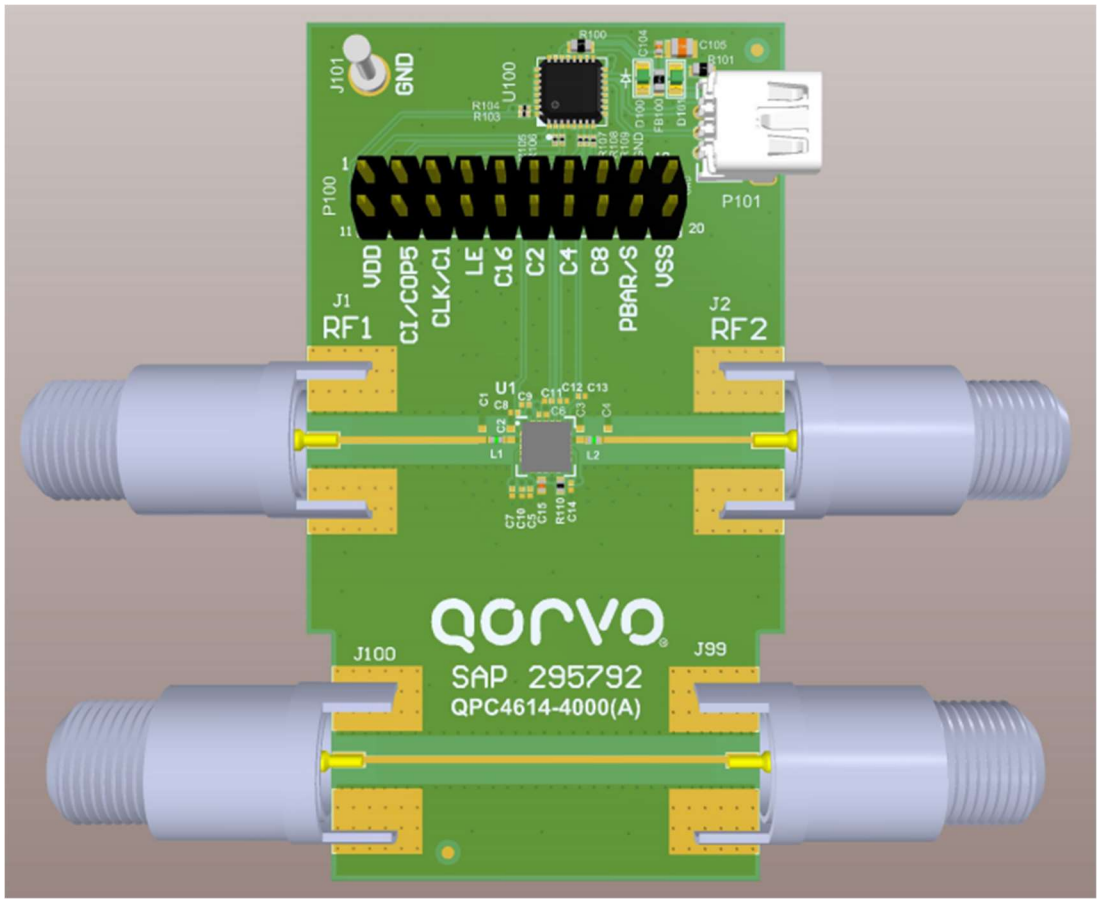
Evaluation Board Schematic; USB Interface



Evaluation Board Bill of Materials

Ref Designator	Qty	Description	Manufacturer	Manufacturer Part #
	1	PCB, QPC4614	TTM Technologies, Inc.	QPC4614-4000(A)
C102, C103	2	CAP, 47pF, 5%, 50V, C0G, 0402	Kamaya, Inc	HH15N470J500CT
C101	1	CAP, 0.01uF, 10%, 50v, X7R, 0402	Murata Electronics	GCM155R71H103KA55D
C105	1	CAP, 4.7uF, 10%, 16V, X7R, 0805	AVX Asia Limited	0805YC475KAT2A
C15, C100, C104	3	CAP, 0.1uF, 10%, 50V, X7R, 0402	TDK Singapore PTE LT	C1005X7R1H104K050BE
L1, L2	2	IND, 3.6nH, +/-0.1nH, M/L, 0402	Murata Electronics	LQG15HS3N6B02D
R100, R101	2	RES, 33K, 5%, 1/10W, 0603	Kamaya, Inc	RMC1/16S-333JTH
R103, R104, R105, R106, R107, R108, R109	7	RES, 0 Ohm, JUMPER, 0201	Kamaya, Inc	RMC1/20JPPA15
R102	3	RES, 0 Ohm, 5%, 1/10W, 0402	Kamaya, Inc	RMC1/16SJPTH
D100, D101	2	LED, GRN, CLR, 3.2V, 30Ma, 0603	Wurth Elektronik	150060GS75000
FB100	1	FER, BEAD, 1K, 100mA, 0603	Murata Electronics	BLM18AG102SN1D
U100	1	IC, USB-ART, 3.3-5.25V, QFN-32	Future Technology Devices Int'l Ltd	FT232RQ-REEL
S1-11, S2-12, S3-13, S4-14, S5-15, S6-16, S7-17, S8-18, S9-19, S10-20	10	JUMPER, 2-Pin	3M Interconnect Solutions	929950-00
P100	1	CONN, HDR, ST, 2x10, 0.100"	Samtec, Inc.	TSW-110-07-G-D
P101	1	CONN, USB, MINI-B, RT, ANG, 5-PIN, T/H	Molex	054819-0519
J1, J2, J99, J100	4	CONN, F FEM EDGE MOUNT, 75 OHMS, 0.065	Genesis Technology USA	GT20-300204
J101	1	862000-055 TERM, SOLDER TURRET, 0.062 PCB	Mouser Electronics, Inc	2533-0-00-44-00-00-07-0
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C106, R110	16	Do Not Populate		

Evaluation Board Assembly Drawing



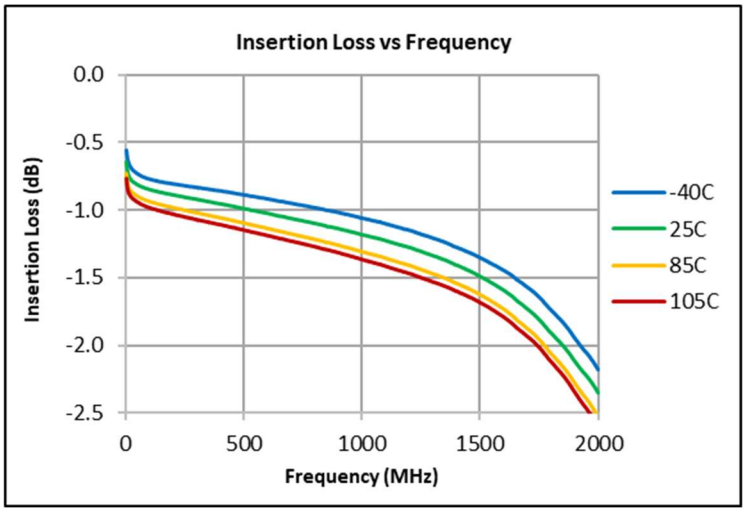
On Board Jumpers (P100)

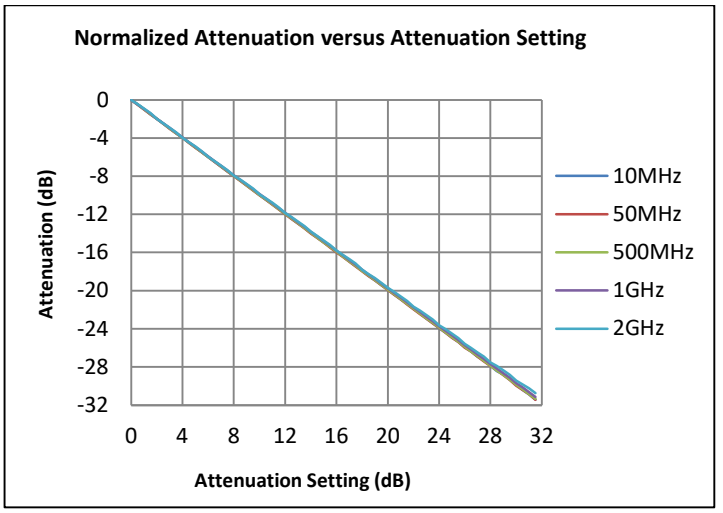
Jumper	Signal	Position	Comment
1-11	VDD	Jumper	Install to supply QPC4614 from USB 3.3V. Remove for external supply from P100-11.
2-12	CI/C0P5	Jumper	Serial Data / Parallel C0.5 Control Line
3-13	CLK/C1	Jumper	Serial Clock / Parallel C1 Control Line
4-14	LE	Jumper	Latch Enable Control Line
5-15	C16	Jumper	Parallel C16 Control Line
6-16	C2	Jumper	Parallel C2 Control Line
7-17	C4	Jumper	Parallel C4 Control Line
8-18	C8	Jumper	Parallel C8 Control Line
9-19	PBAR/SI	Open (Pin to Pull-up Resistor)	Serial Mode
		Jumper (Pin to GND)	Parallel Mode
10-20	VSS – Negative Source	Jumper	Use to tie VSS to GND to enable internal Negative Voltage Generator (NVG), or remove jumper to disable internal NVG and apply -5V.

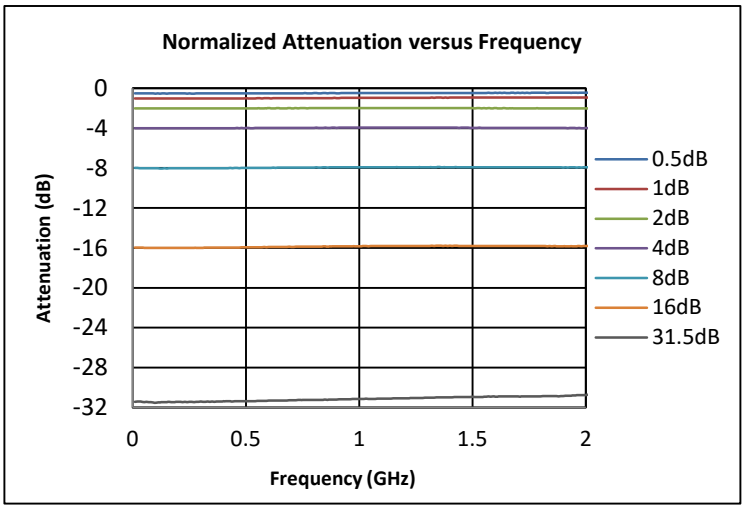
Note: Attenuator is internally controlled and powered, through the USB port, when all jumpers are applied (3.3V).

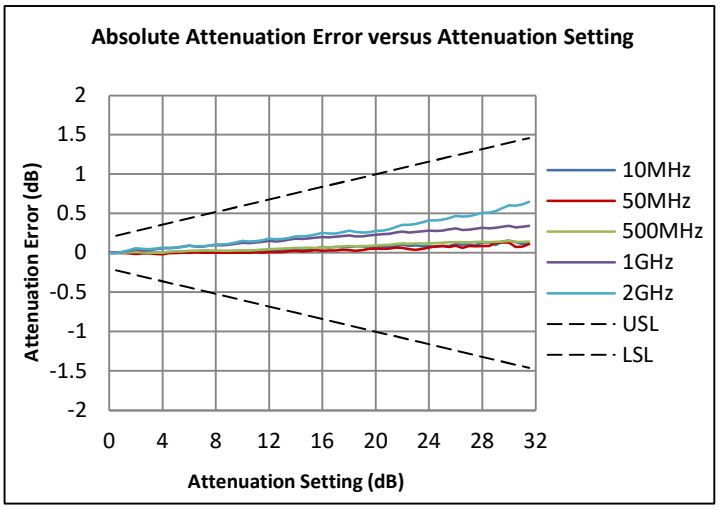
Performance Plots

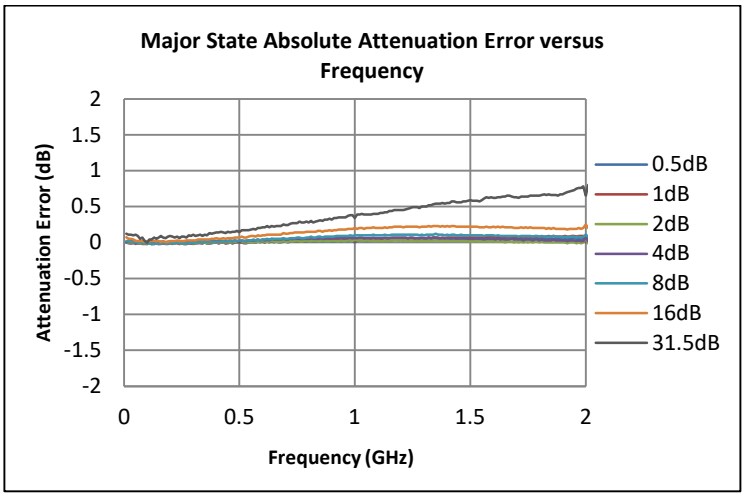
Test conditions unless otherwise noted: Vdd = +5V, Vss = 0V, Temp = +25C, Zo = 75Ω

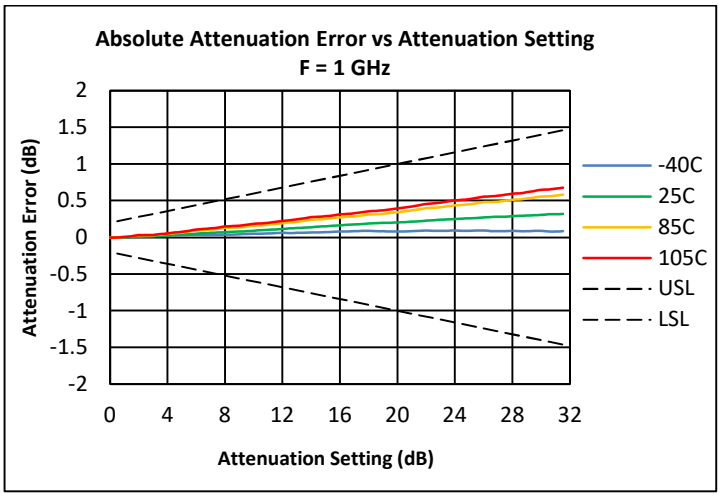






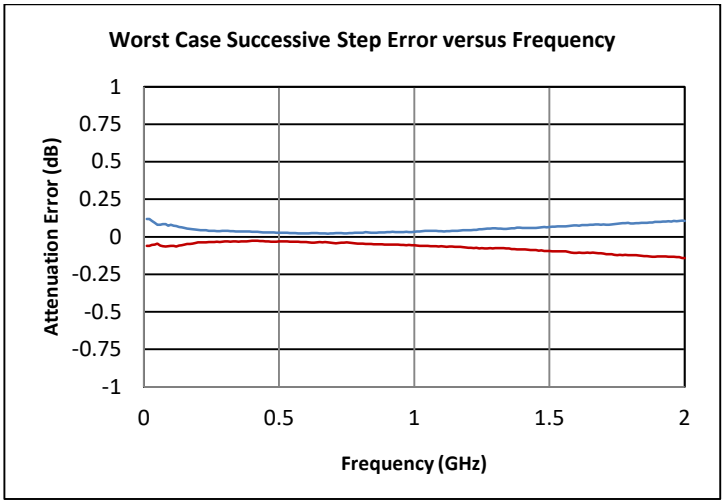


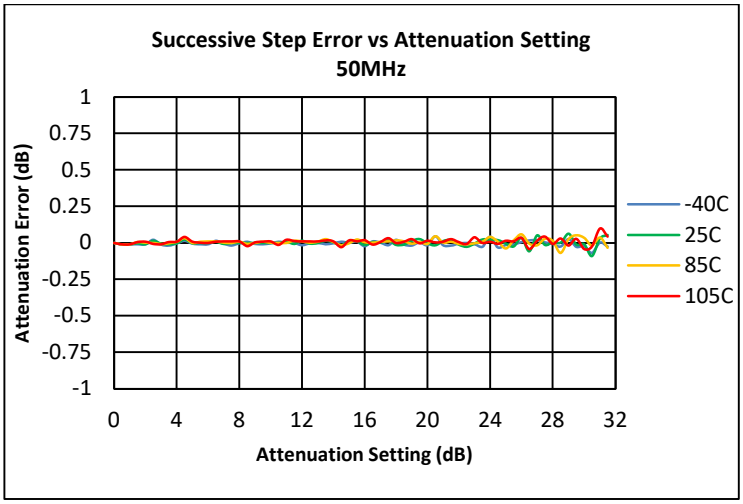


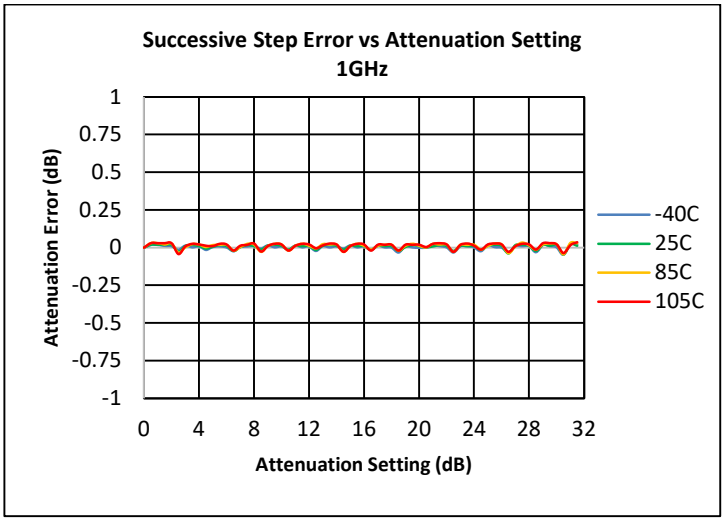


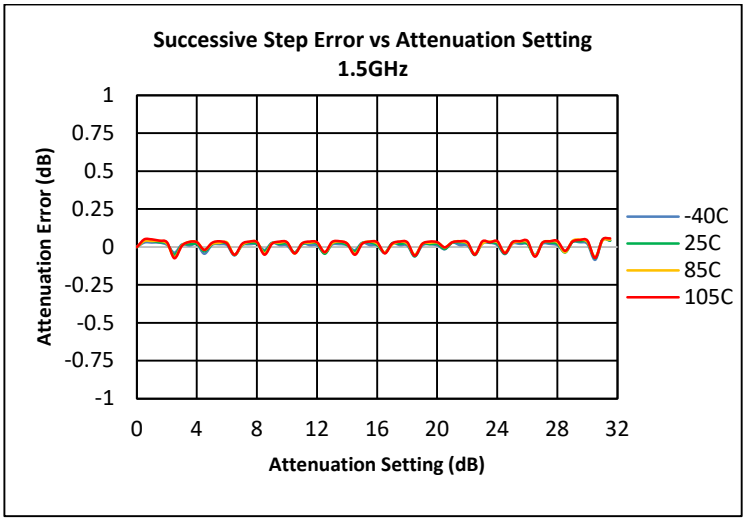
Performance Plots (cont'd.)

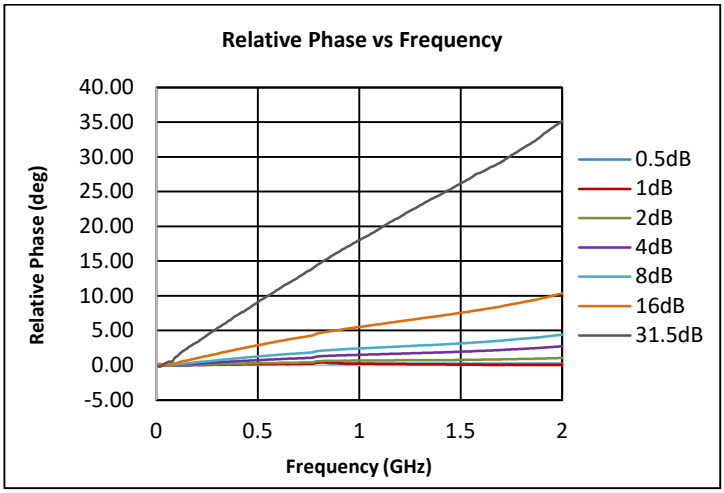
Test conditions unless otherwise noted: Vdd = +5V, Vss = 0V, Temp = +25C, Zo = 75Ω

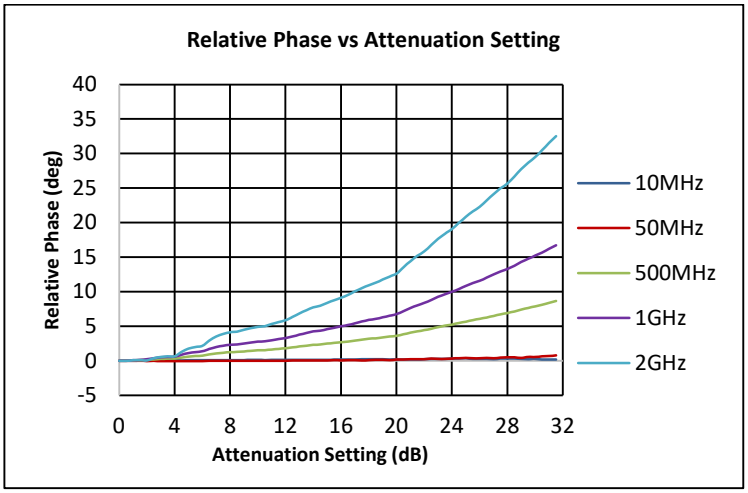






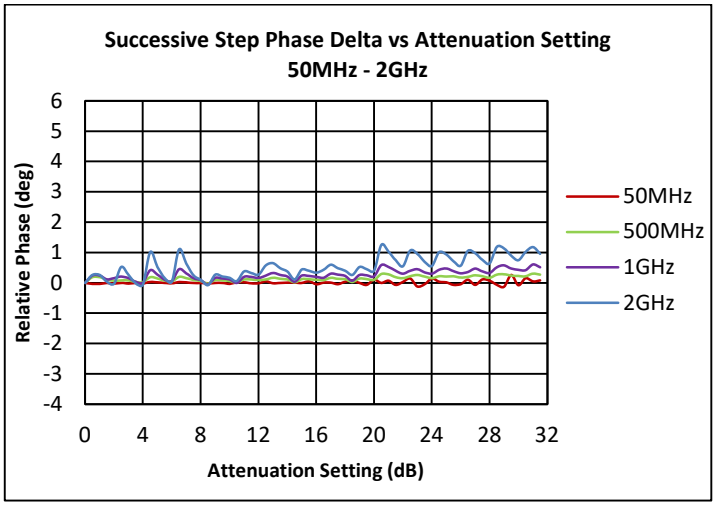


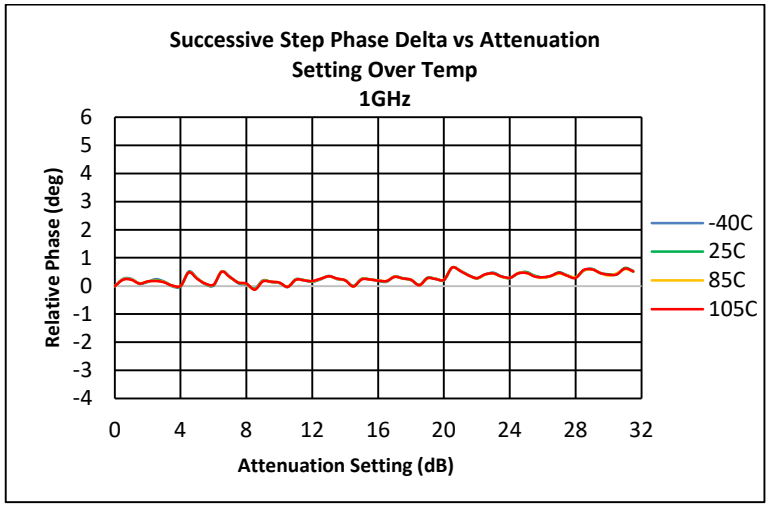


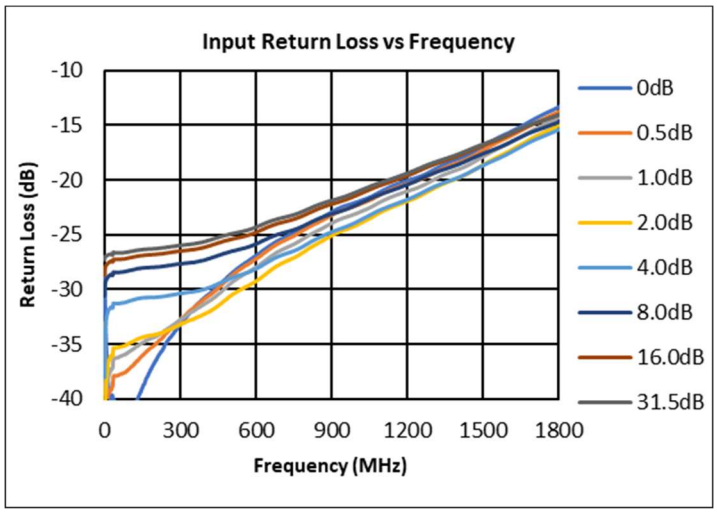


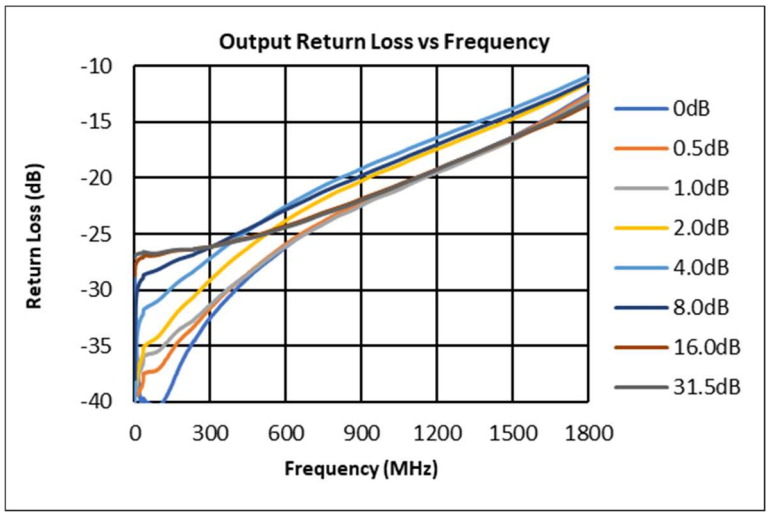
Performance Plots (cont'd.)

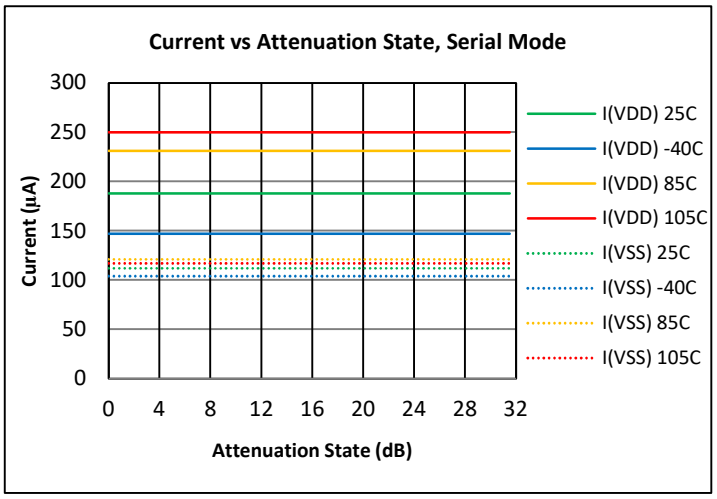
Test conditions unless otherwise noted: Vdd = +5V, Vss = 0V, Temp = +25C, Zo = 75Ω

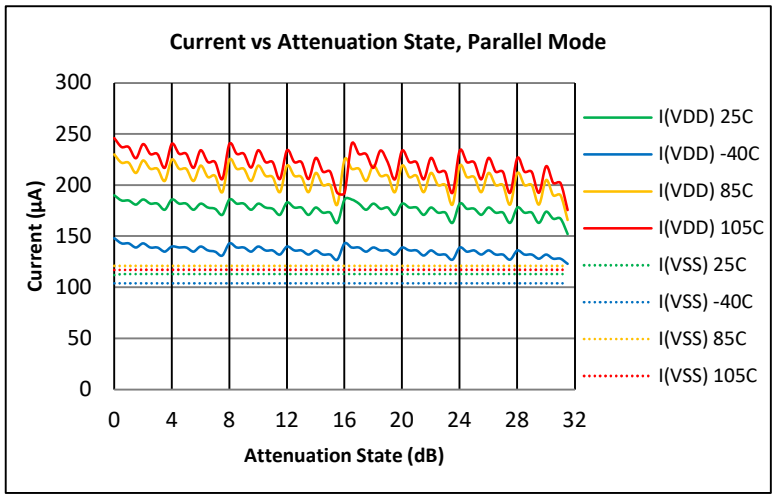






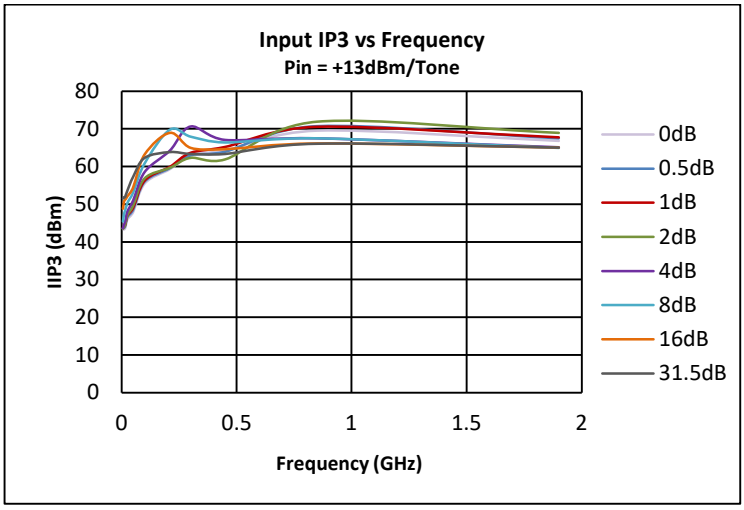


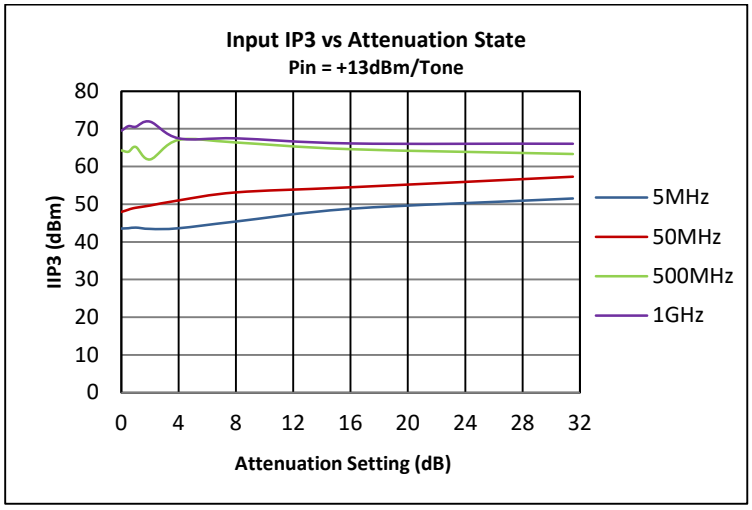


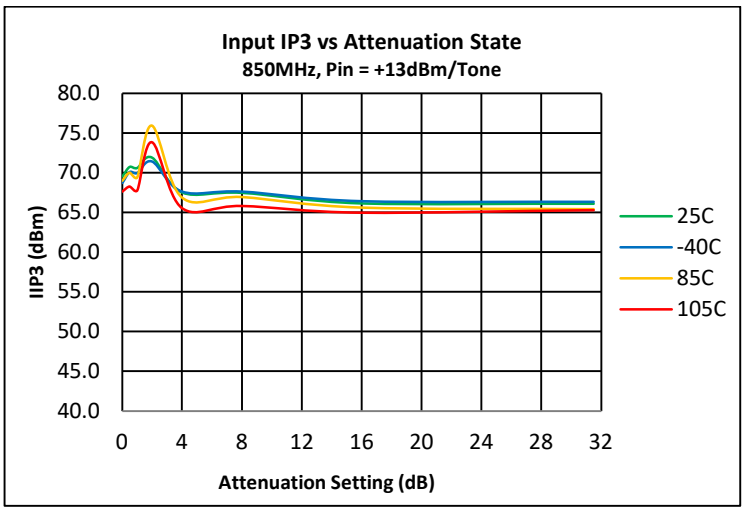


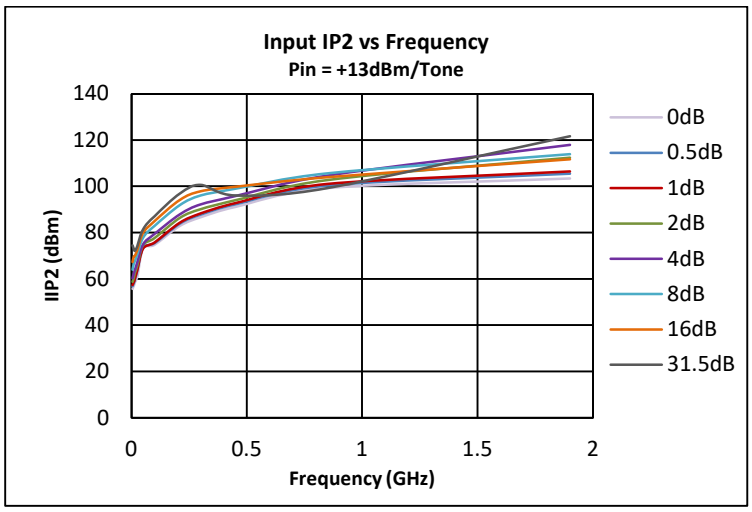
Performance Plots (cont'd.)

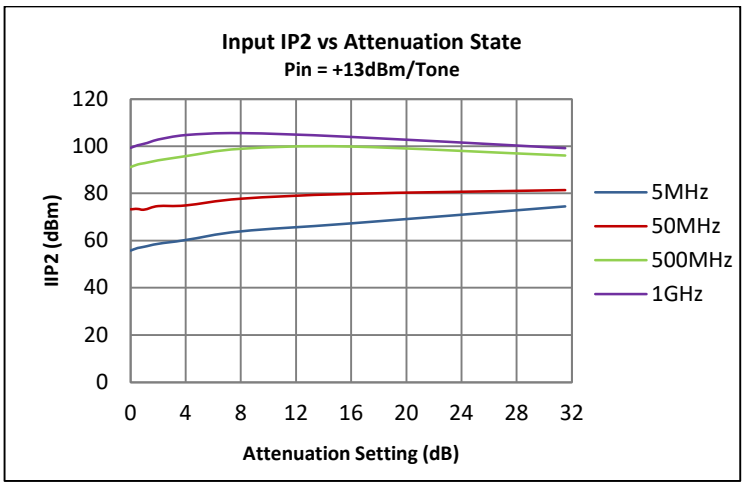
Test conditions unless otherwise noted: Vdd = +5V, Vss = 0V, Temp = +25C, Zo = 75Ω

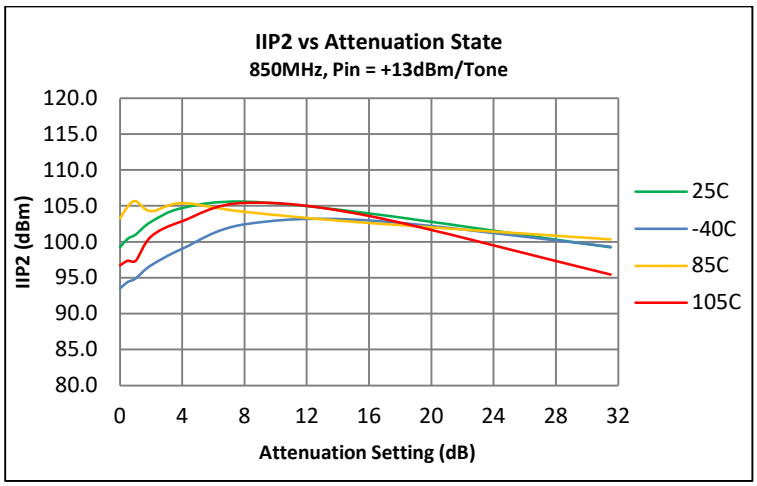






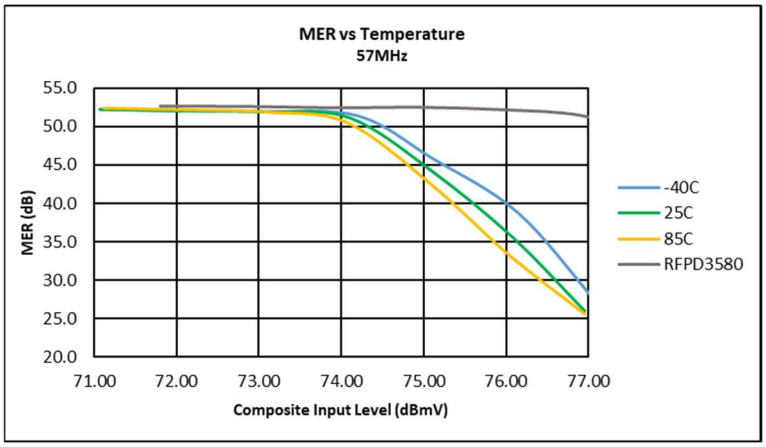


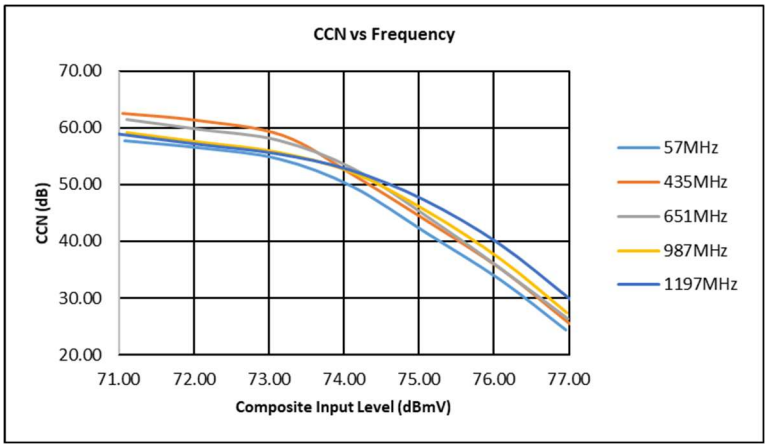


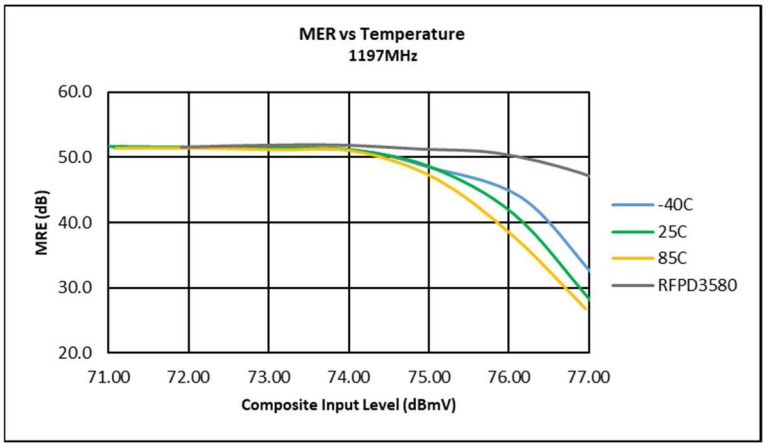


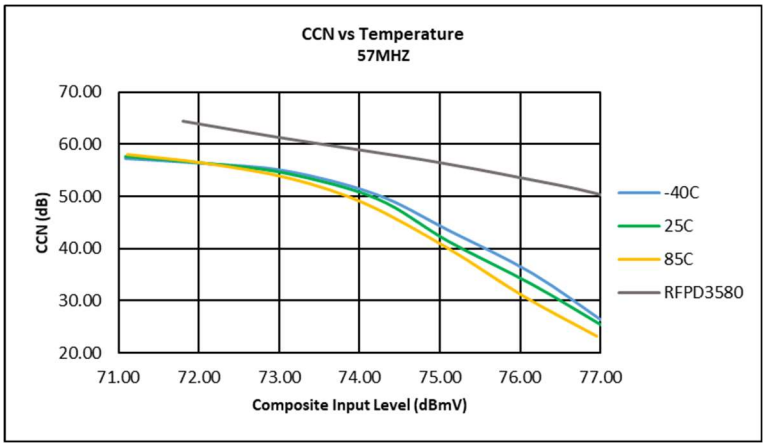
Performance Plots (cont'd.)

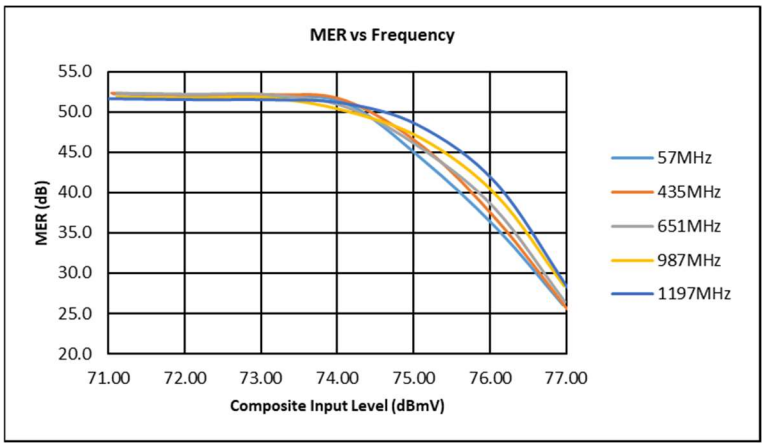
Test conditions unless otherwise noted: Vdd = +5V, Vss = 0V, Temp = +25C, Zo = 75Ω

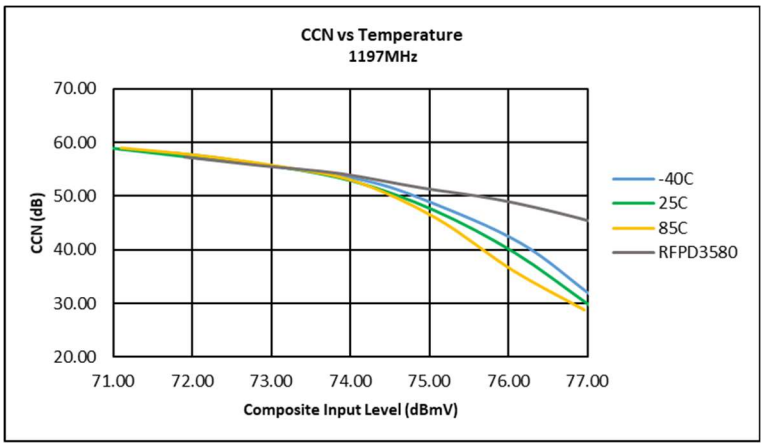








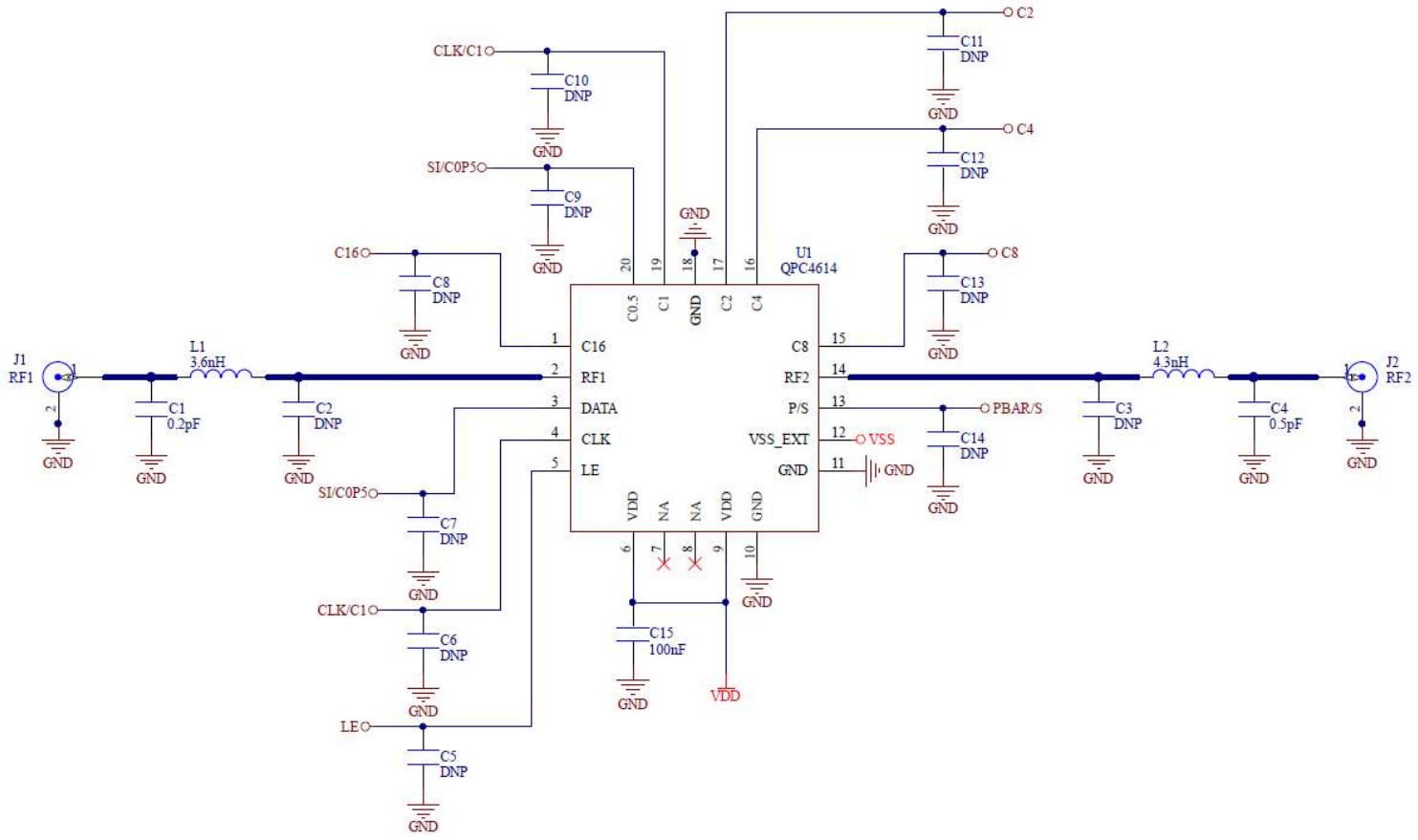




MER/CCN Test Conditions:

1. 190 QAM256 Channels, 57-1215MHz, ITU-T J.83, Annex B, Flat Tilt
2. MER Source corrected. Maximum Source Correction, 4.3dB
3. CCN test procedure according to ANSI/SCTE 17, System BW = 5.36MHz
4. 0dB attenuation setting

Additional Applications; 1.8GHz Improved Return Loss



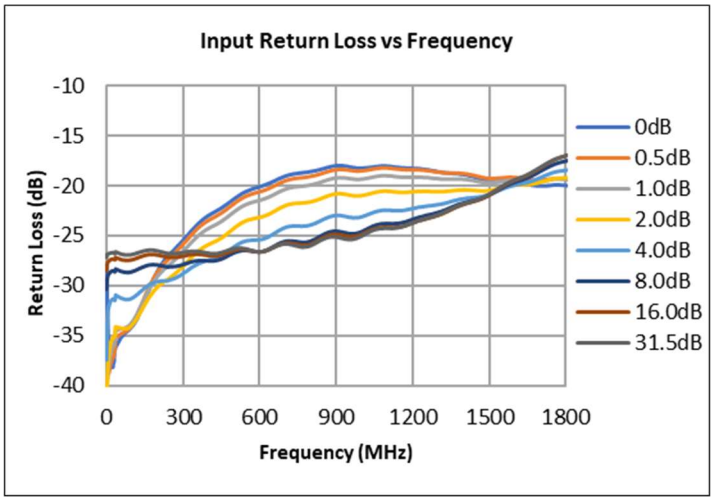
BOM Changes for extended bandwidth:			
L1	3.6nH	Murata	LQG15HS3N6B02D
L2	4.3nH	Murata	LQG15HS4N3B02D
C1	0.2pF	Murata	GJM1555C1HR20WB01D
C4	0.5pF	Murata	GJM1555C1HR50WB01D

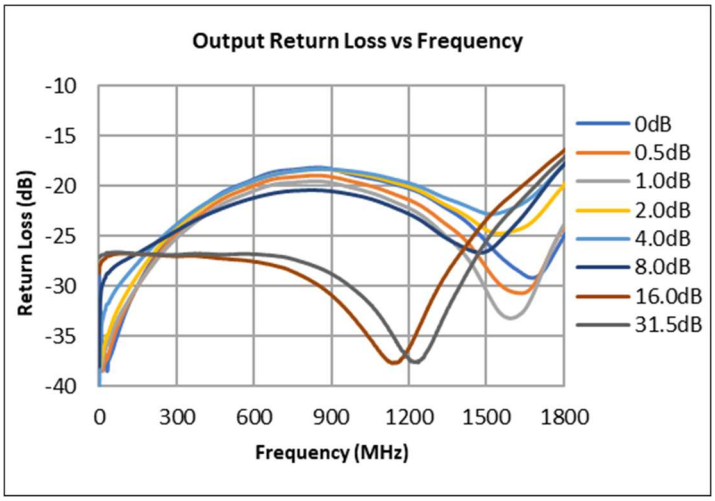
Notes:

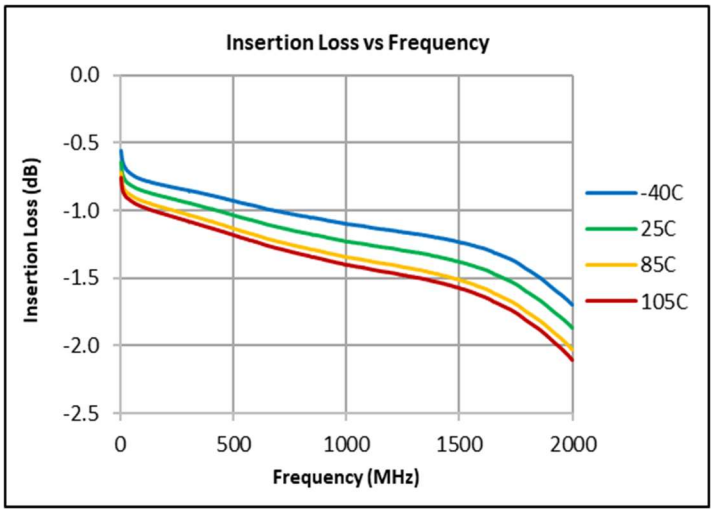
1. 1.8GHz performance can be improved by addition of tuning capacitors C1, C4 and adjusting L1, L2 to balance return loss at all states.
2. Final tuning of values may be required in the application circuit or may be optimized for preferred operating attenuation ranges.
3. De-embedded S-parameters available upon request to aid in simulations and final tuning.

Additional Applications, 1.8GHz Improved Return Loss (cont'd.)

Test conditions unless otherwise noted: Vdd = +5V, Vss = 0V, Temp = +25C, Zo = 75Ω







Evaluation Board Programming Using USB Interface

Serial Mode
All programming jumpers on the evaluation board are installed as indicated in the table on page 6, except jumper 9-19,which is removed to set QPC4614 in serial mode. Power for QPC4614 is supplied from USB unless Jumper 1-11 is removed to apply an external VDD. Refer to the Control Bit Generator (CBG) Software Reference Manual for instructions on how to setup the software for use. Select 'QPC4614' for serial operation from the parts list of the CBG user interface. Set the attenuation value using the CBG user interface.

Direct Parallel Mode
All programming jumpers on the evaluation board are installed as indicated in the table on page 6. Jumper 19-9 is installed in this case to set QPC4614 in parallel mode. Power for QPC4614 is supplied from USB unless Jumper 1-11 is removed to apply an external VDD. Refer to the Control Bit Generator (CBG) Software Reference Manual for instructions on how to setup the software for use. Select 'QPC4614-P' from the parts list of the CBG user interface. Set the attenuation value using the CBG user interface.

Evaluation Board Programming Using External Bus

Serial Mode
For external control, remove all jumpers from P100 and connect a user-supplied harness on the QPC4614 side of P100 (pins 11-20). Apply the appropriate VDD, CLK, Data, LE, and GND signals to P100. Jumper 10-20 should be installed to enable the internal NVG unless an external -5V supply is applied to pin 20. Send the appropriate signals onto the serial bus lines in accordance with the Serial Mode Timing Diagram.

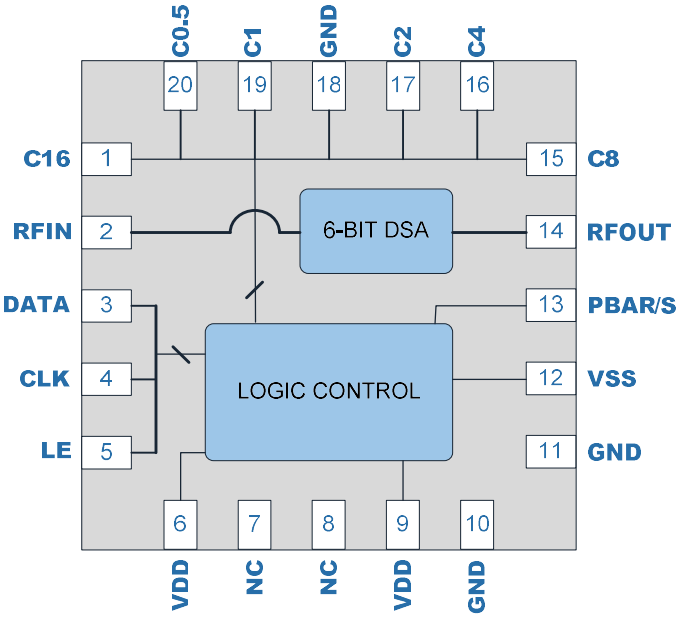
Latched Parallel Mode
Latched Parallel Mode holds the current attenuation state while the LE line remains low. Pulsing the LE control high will latch the internal registers to the state of the control line inputs and update the attenuation state. To operate in latched parallel mode with external controls, remove all jumpers except 9-19 (sets QPC4614 in parallel mode) and connect a user-supplied harness on the QPC4614 side of P100 (pins 11-20). Apply the appropriate VDD, C16 – C0.5, LE, and GND signals. Jumper 10-20 should be installed to enable the internal NVG unless an external -5V supply is applied to pin 20. Send the appropriate parallel control and LE signals in accordance with the Latched Parallel Mode Timing Diagram.

Direct Parallel Mode
In Direct Parallel Mode, the LE signal is held at logic high so that the attenuation will change state immediately when there is a change in logic state for any of the parallel bus signals, C16 – C0.5. Remove all jumpers except 9-19 (sets QPC4614 in parallel mode) and connect a user-supplied harness on the QPC4614 side of P100 (pins 11-20). Apply the appropriate VDD, C16 – C0.5 and GND signals. Jumper 10-20 should be installed to enable the internal NVG unless an external -5V supply is applied to pin 20.

Default Power-up State

This default attenuation state is maximum (31.5 dB) when supply voltage is applied to the attenuator in both serial and parallel modes. If a different attenuation state is desired during power-up, apply signals according to the Parallel Mode Truth Table to the C0.5 – C16 pins. The attenuator will power-up to the state applied to the parallel bus during turn on. The LE signal must be held to logic '0' during power-up.

Pin Configuration and Description



Top View

Pin	Label	Description
1	C16	16dB Parallel Control Bit
2	RFIN	RF Input Pin: Incident RF power must enter this pin for rated thermal performance and reliability. Do not apply DC power to this pin. Pin may be DC grounded externally and is grounded through resistors.
3	DATA	Serial Bus Data Input
4	CLK	Serial Bus Clock Input
5	LE	Latch Enable: The leading edge of signal on LE causes the attenuator to change state for serial and latched parallel modes. For direct parallel mode keep LE at logic high level.
6	VDD	Supply Voltage
7	NC	No Connection
8	NC	No Connection
9	VDD	Supply Voltage
10	GND	Ground Pin
11	GND	Ground Pin
12	VSS	External Negative Supply Voltage. Ground VSS pin to use internal negative voltage generator.
13	PBAR/S	Mode Select Pin, Logic Low = Parallel, Logic High = Serial
14	RFOUT	RF Output Pin: Pin may be DC grounded externally and is grounded thru resistors internal to the part.
15	C8	8dB Parallel Control Bit
16	C4	4dB Parallel Control Bit
17	C2	2dB Parallel Control Bit
18	GND	Ground Pin
19	C1	1dB Parallel Control Bit
20	C0.5	0.5dB Parallel Control Bit
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

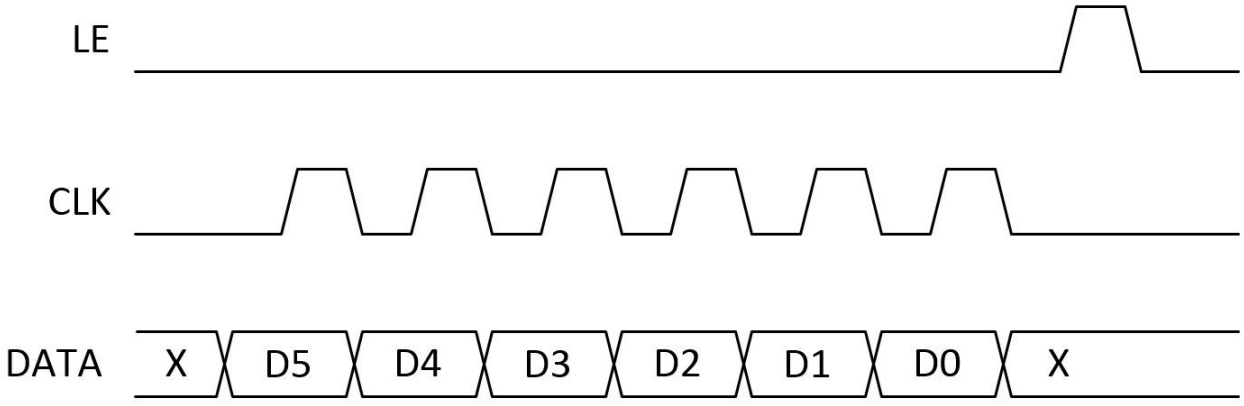
Serial Mode Attenuation Word Truth Table

Attenuation Word							Attenuation State
D5	D4	D3	D2	D1	D0 (LSB)		
L	L	L	L	L	L		0 dB / Reference Insertion Loss
L	L	L	L	L	H		0.5 dB
L	L	L	L	H	L		1 dB
L	L	L	H	L	L		2 dB
L	L	H	L	L	L		4 dB
L	H	L	L	L	L		8 dB
H	L	L	L	L	L		16 dB
H	H	H	H	H	H		31.5 dB

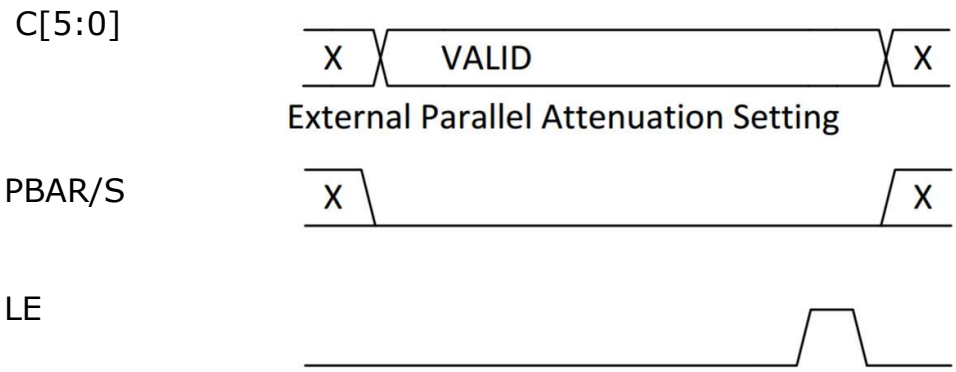
Parallel Mode Attenuation Word Truth Table

Attenuation Word							Attenuation State
C16	C8	C4	C2	C1	C0.5 (LSB)		
L	L	L	L	L	L		0 dB / Reference Insertion Loss
L	L	L	L	L	H		0.5 dB
L	L	L	L	H	L		1 dB
L	L	L	H	L	L		2 dB
L	L	H	L	L	L		4 dB
L	H	L	L	L	L		8 dB
H	L	L	L	L	L		16 dB
H	H	H	H	H	H		31.5dB

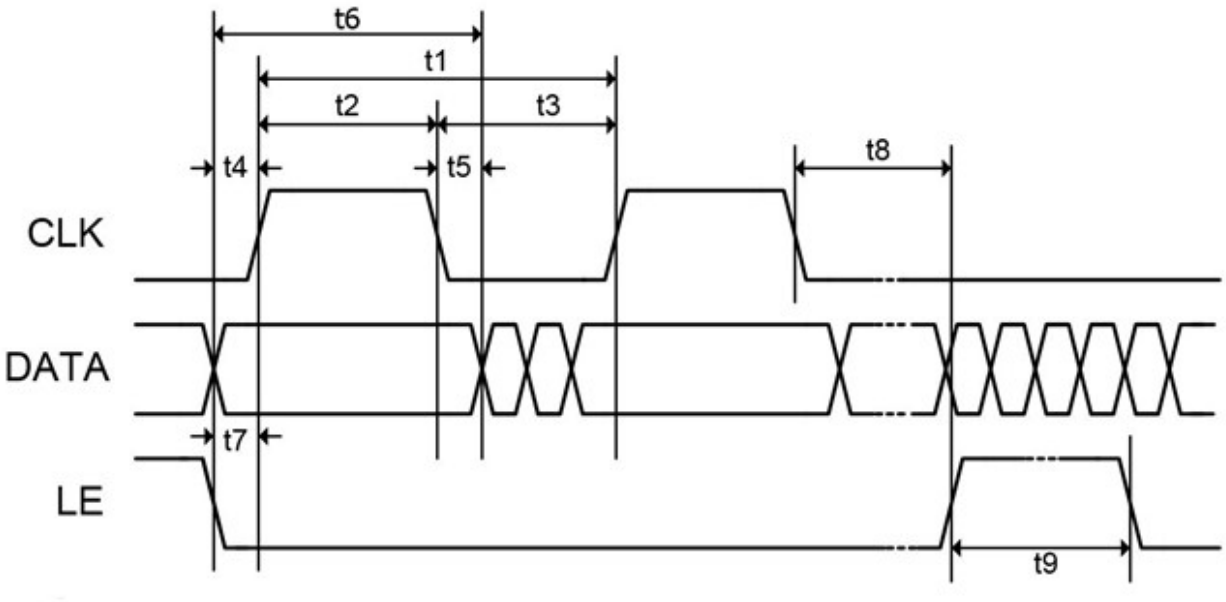
Serial Mode Timing Diagram



Latched Parallel Mode Timing Diagram

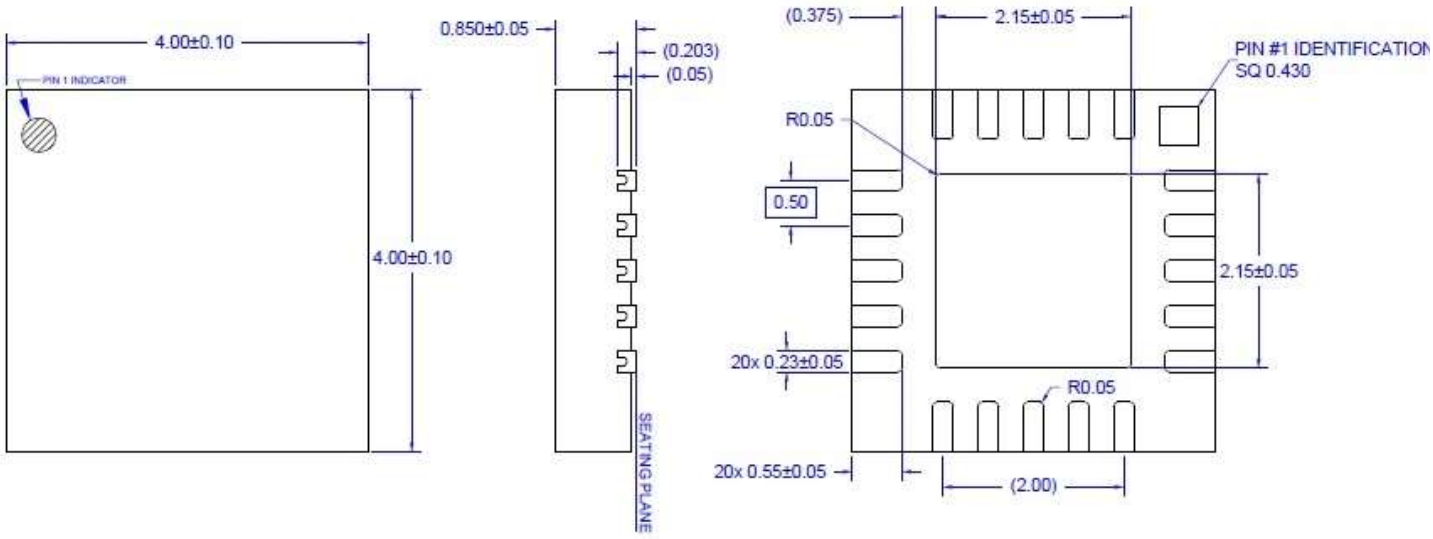


Serial BUS Timing Specifications



Parameter	Limit	Unit	Comment
t1	25	MHz max	CLK Frequency
t2	20	ns min	CLK High
t3	20	ns min	CLK Low
t4	5	ns min	Data to CLK Setup Time
t5	5	ns min	Data to CLK Hold Time
t6	30	ns min	Data Valid
t7	5	ns min	LE to CLK Setup Time
t8	5	ns min	CLK to LE Setup Time
t9	10	ns min	LE Pulse Width

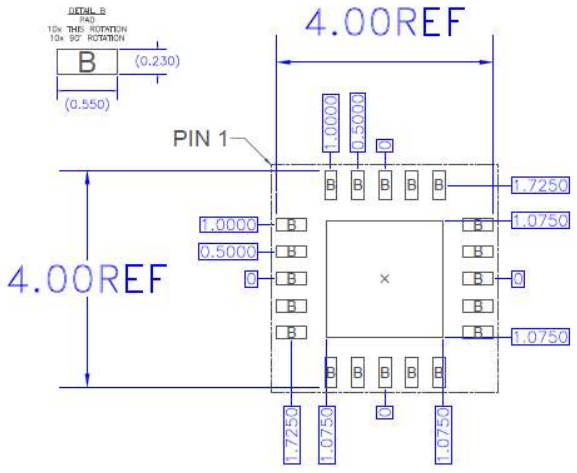
Package Dimensions



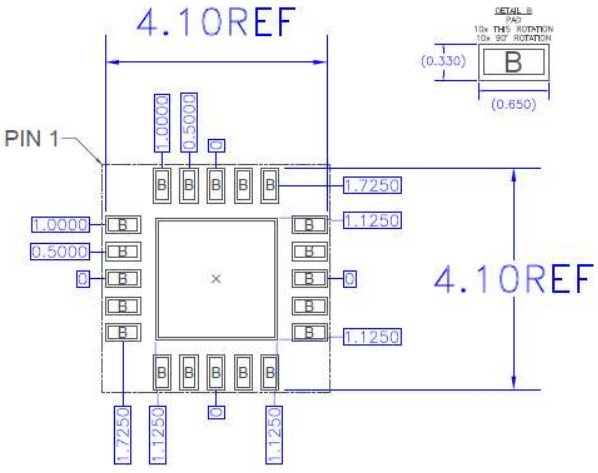
20 Pin 4 x 4mm QFN Package

Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
4. Contact plating: NiPdAu

Recommended Mounting Pattern

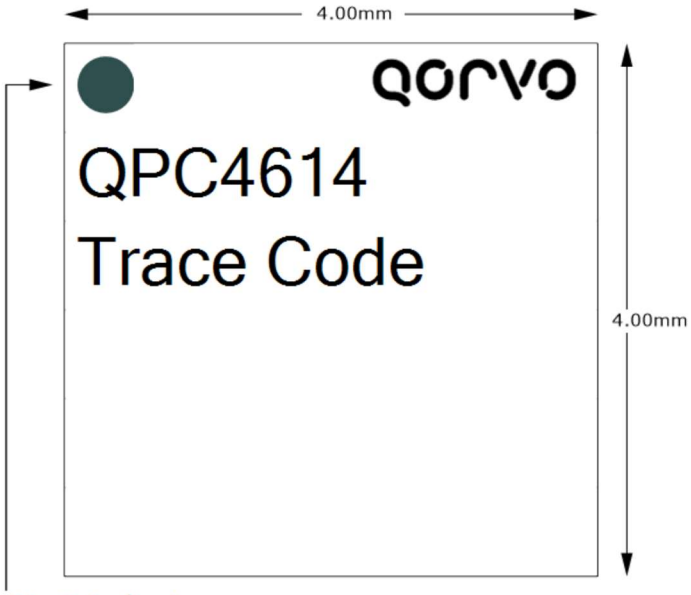


RECOMMENDED
LAND PATTERN



RECOMMENDED
LAND PATTERN MASK

Package Marking



Pin 1 Indicator
Qorvo Logo - Use Qo5D
Trace Code to be assigned by subcon

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C (1500V)	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3 (1500V)	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 2	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: **1-844-890-8163**

Web: www.qorvo.com

Email: customer.support@qorvo.com

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