IRS21867S

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Low VCC operation
- Gate drive supply range from 6.8 V to 20 V
- Undervoltage lockout for both channels
- 3.3V and 5V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5 V offset
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability 4.0 A (Typ.)
- Leadfree, RoHS compliant

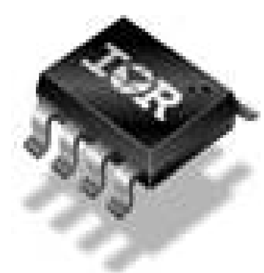
Applications

- Battery powered equipment
- Hand-tools
- Fork-lifts
- Golf-carts
- RC Hobby Equipment
- E-bike

Product Summary

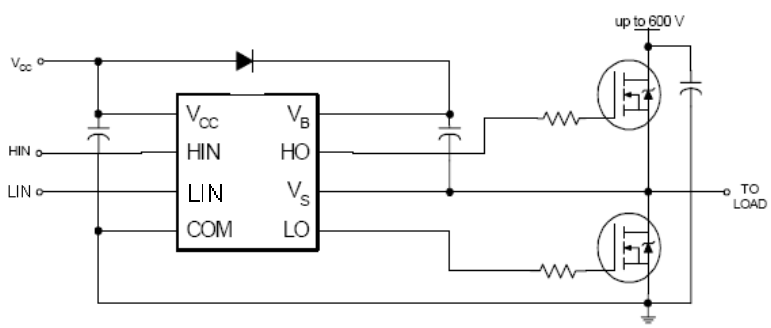
Topology	Single-Phase
V_{OFFSET}	≤ 600 V
V_{OUT}	6.8 V – 20 V
I_{o+} & I_{o-} (typical)	4.0 A & 4.0 A
t_{on} & t_{off} (typical)	170 ns & 170 ns

Package Options



SOIC-8

Typical Connection Diagram



IRS21867S

Refer to Lead Assignment for correct pin Configuration. This diagrams show electrical Connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout

Description

The IRS21867 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Low VCC operation allows use in battery powered applications. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600V.

Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC8N	MSL2††† 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class A (per JEDEC standard JESD22-A115)	
	Human Body Model	Class 2 (per EIA/JEDEC standard EIA/JESD22-A114)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min	Max	Units
V_B	High side floating absolute voltage	-0.3	625 (Note 1)	V
V_S	High side floating supply offset voltage	V_B – 25	V_B + 0.3	
V_{HO}	High side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage	-0.3	25 (Note 1)	
V_{LO}	Low side output voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN)	COM - 0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient	—	50	V/ns
P_D	Package power dissipation @ TA ≤ 25°C	—	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient	—	200	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-50	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Note 1: All supplies are fully tested at 25V.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The V_S offset rating is tested with all supplies biased at (VCC-COM) = 15V.

Symbol	Definition	Min	Max	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 2	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	6.8	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN)	COM	V_{CC}	
T_A	Ambient temperature	-40	125	°C

† Note 2: Logic operational for V_S of -5V to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{CC} = V_{BS} = 15V, C_L = 1000 pF, T_A = 25°C unless otherwise specified.

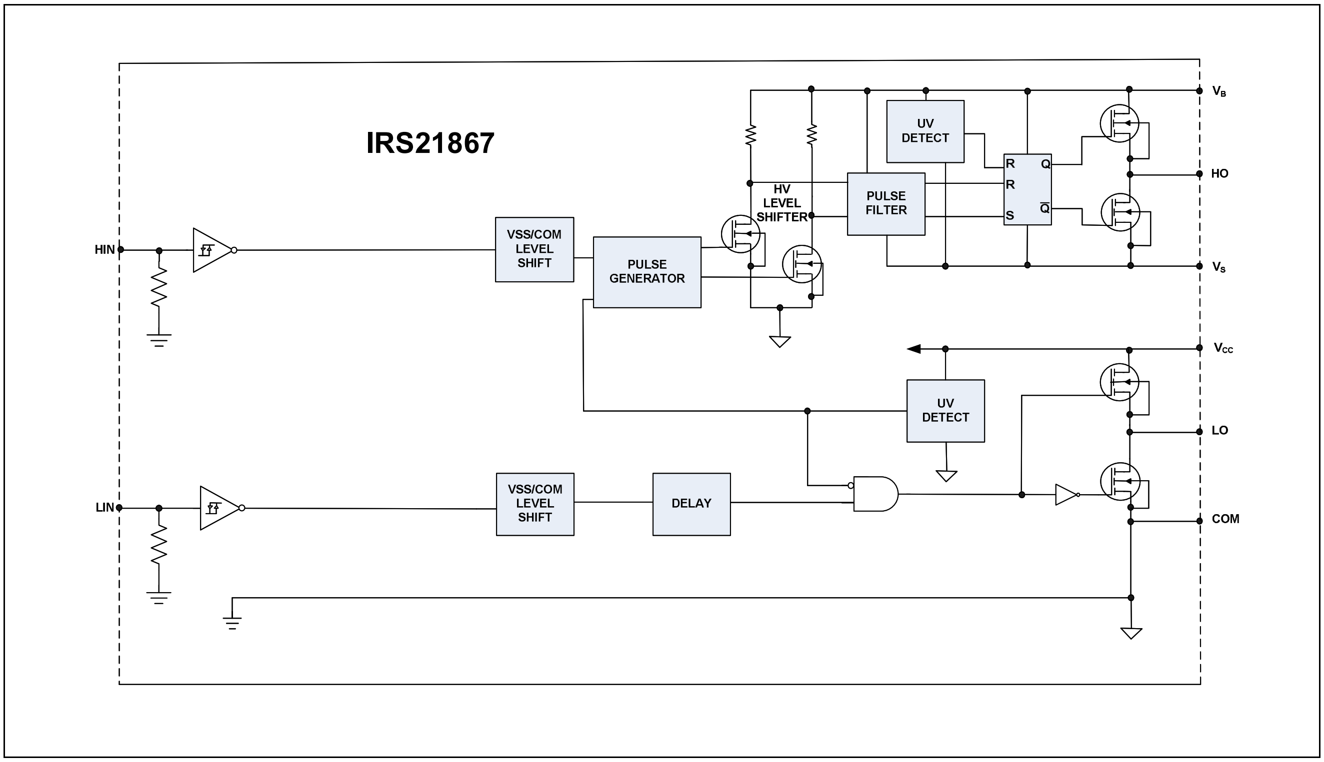
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	170	250	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	170	250		V_S = 0V or 600V
MT	Delay matching | t_{on} – t_{off} |	—	—	35		
t_r	Turn-on rise time	—	22	38		V_S = 0V
t_f	Turn-off fall time	—	18	30		

Static Electrical Characteristics

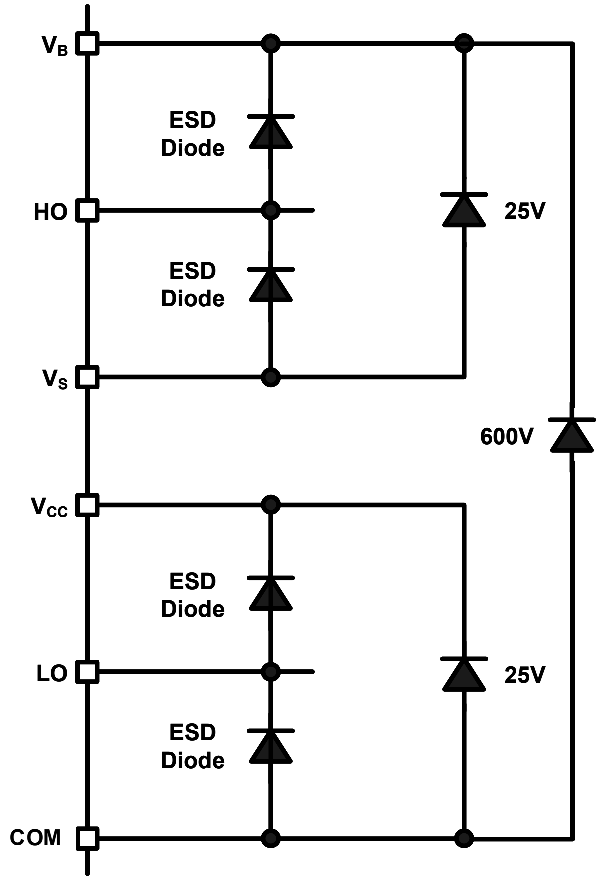
V_{CC} = V_{BS} = 15V,, and T_A = 25°C unless otherwise specified. The V_{IN}, and I_{IN} parameters are referenced to COM and are applicable to the respective input leads: HIN, and LIN. The V_O, and I_O parameters are referenced to V_S/COM and are applicable to the respective output leads: HO and LO.

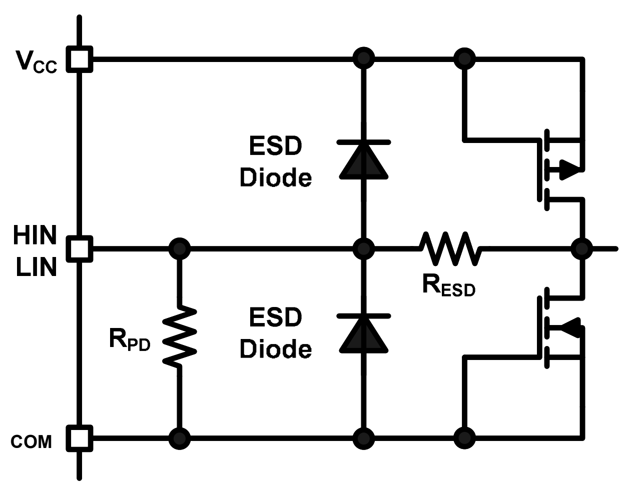
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HO & LO	2.5	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic "0" input voltage for HO & LO	—	—	0.8		
V_{OH}	High level output voltage, V_{CC} or V_{BS} - V_O	—	—	1.4		I_O = 0mA
V_{OL}	Low level output voltage, V_O	—	—	0.15		I_O = 20mA
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	50	120	240		
I_{IN+}	Logic "1" input bias current	—	250	—		HIN = LIN = 5V
I_{IN-}	Logic "0" input bias current	—	—	5.0		HIN = LIN = 0V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	5.34	6	6.66	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	4.90	5.50	6.10		
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage Hysteresis		0.5			
I_{O+}	Output high short circuit pulsed current		4.0		A	V_O = 0V, PW ≤ 10µs
I_{O-}	Output low short circuit pulsed current		4.0			V_O = 15V, PW ≤ 10µs

Functional Block Diagrams



Input/Output Pin Equivalent Circuit Diagrams

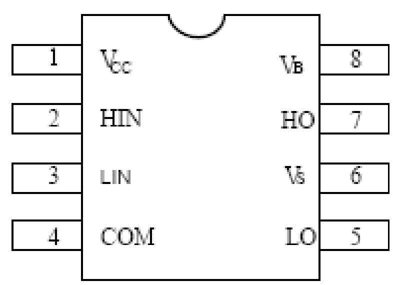




Lead Definitions: IRS21867S

Pin#	Symbol	Description
1	V_{CC}	Low-side and logic fixed supply
2	HIN	Logic input for high-side gate driver output (HO), in phase with HO
3	LIN	Logic input for low-side gate driver output (LO), in phase with LO
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V_S	High-side floating supply return
7	HO	High-side gate drive output
8	V_B	High-side floating supply

Lead Assignments



8 lead SOIC

IRS21867S

Application Information and Additional Details

Informations regarding the following topics are included as subsections within this section of the datasheet.

- IGBT/MOSFET Gate Drive
- Switching and Timing Relationships
- Matched Propagation Delays
- Input Logic Compatibility
- Undervoltage Lockout Protection
- Negative V_S Transient SOA
- PCB Layout Tips
- Additional Documentation

IGBT/MOSFET Gate Drive

The IRS21867 HVIC is designed to drive MOSFET or IGBT power devices. Figures 1 and 2 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{HO} for the high-side power switch and V_{LO} for the low-side power switch; this parameter is sometimes generically called V_{OUT} and in this case does not differentiate between the high-side or low-side output voltage.

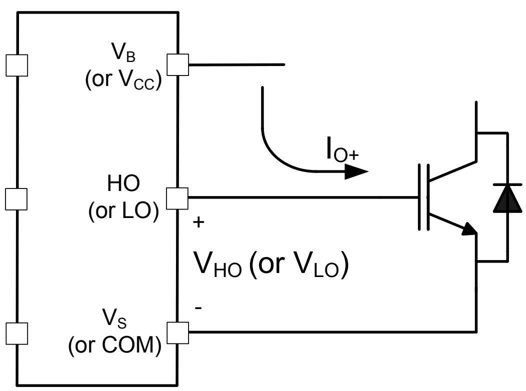


Figure 1: HVIC sourcing current

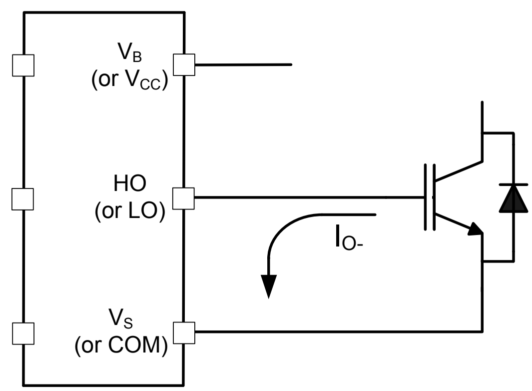


Figure 2: HVIC sinking current

Switching and Timing Relationships

The relationships between the input and output signals of the IRS21867 are illustrated below in Figures 3, 4. From these figures, we can see the definitions of several timing parameters (i.e., PW_{IN}, PW_{OUT}, t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

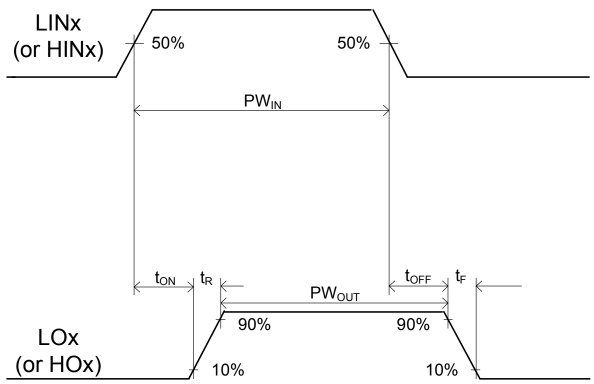


Figure 3: Switching time waveforms

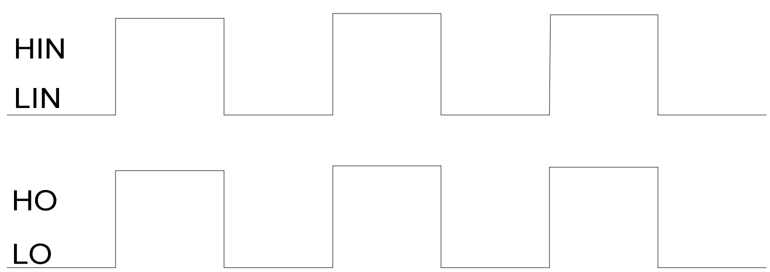


Figure 4: Input/output timing diagram

Matched Propagation Delays

The IRS21867 is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). The propagation turn-on delay (t_{ON}) is matched to the propagation turn-on delay (t_{OFF}).

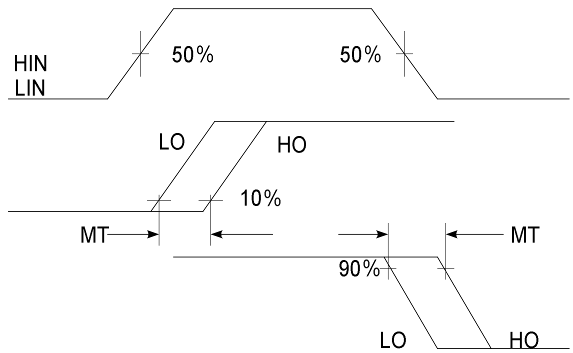


Figure 5: Delay Matching Waveform Definition

Input Logic Compatibility

The inputs of this IC are compatible with standard CMOS and TTL outputs. The IRS21867 has been designed to be compatible with 3.3 V and 5 V logic-level signals. Figure 8 illustrates an input signal to the IRS22867, its input threshold values, and the logic state of the IC as a result of the input signal.

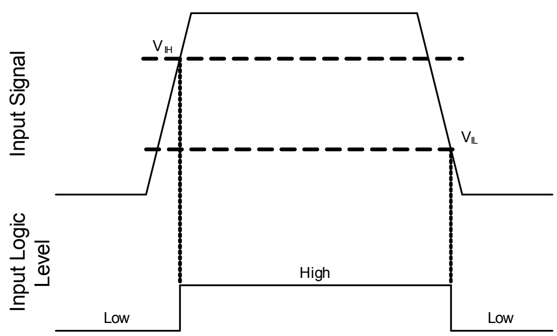


Figure 6: HIN & LIN input thresholds

Undervoltage Lockout Protection

This IC provides undervoltage lockout protection on both the V_{CC} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 7 is used to illustrate this concept; V_{CC} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the IC will not turn-on. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high- and low-side gate drive outputs.

Upon power-up, should the V_{BS} voltage fail to reach the V_{BSUV} threshold, the IC will not turn-on. Additionally, if the V_{BS} voltage decreases below the V_{BSUV} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

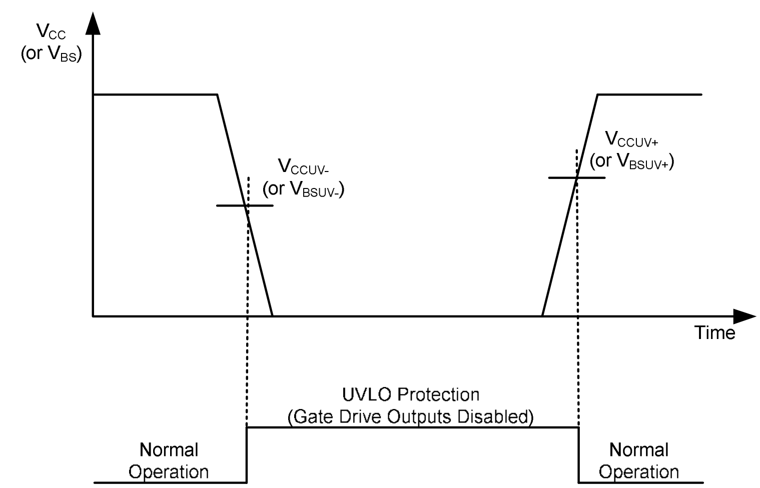


Figure 7: UVLO protection

Tolerant to Negative V_S Transients

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 8; here we define the power switches and diodes of the inverter.

If the high-side switch (e.g., the IGBT Q1 in Figures 9 and 10) switches off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

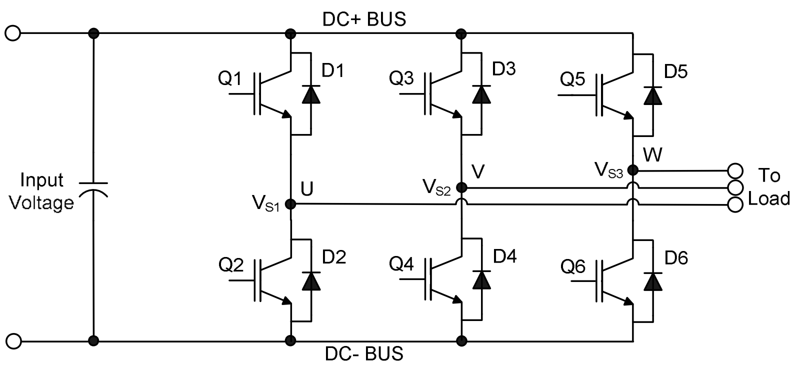


Figure 8: Three phase inverter

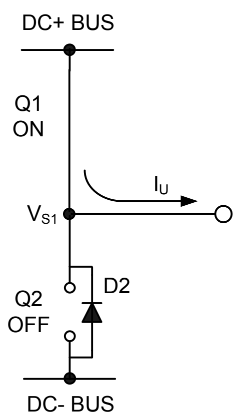


Figure 9: Q1 conducting

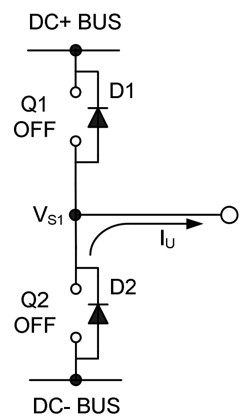


Figure 10: D2 conducting

Also when the V phase current flows from the inductive load back to the inverter (see Figures 11 and 12), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

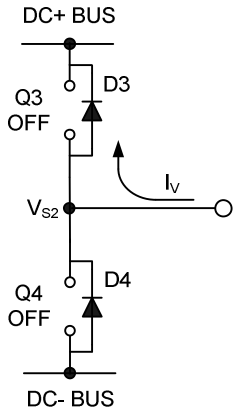


Figure 11: D3 conducting

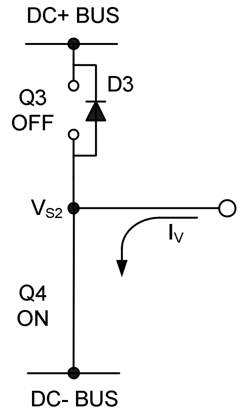


Figure 12: Q4 conducting

However, in a real inverter circuit, the V_S voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called "negative V_S transient".

The circuit shown in Figure 13 depicts one leg of the three phase inverter; Figures 14 and 15 show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

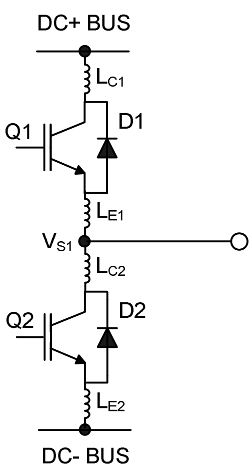


Figure 13: Parasitic Elements

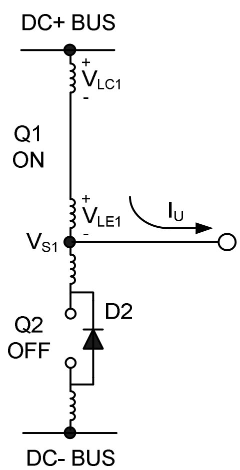


Figure 14: V_S positive

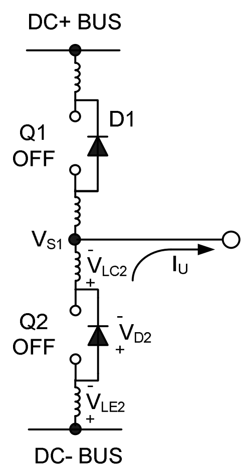


Figure 15: V_S negative

In a typical motor drive system, dV/dt is typically designed to be in the range of 3-5 V/ns. The negative V_S transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

International Rectifier's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the IRS21867's robustness can be seen in Figure 16, where there is represented the IRS21867 Safe Operating Area at V_{BS}=15V based on repetitive negative V_S spikes. A negative V_S transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside SOA.

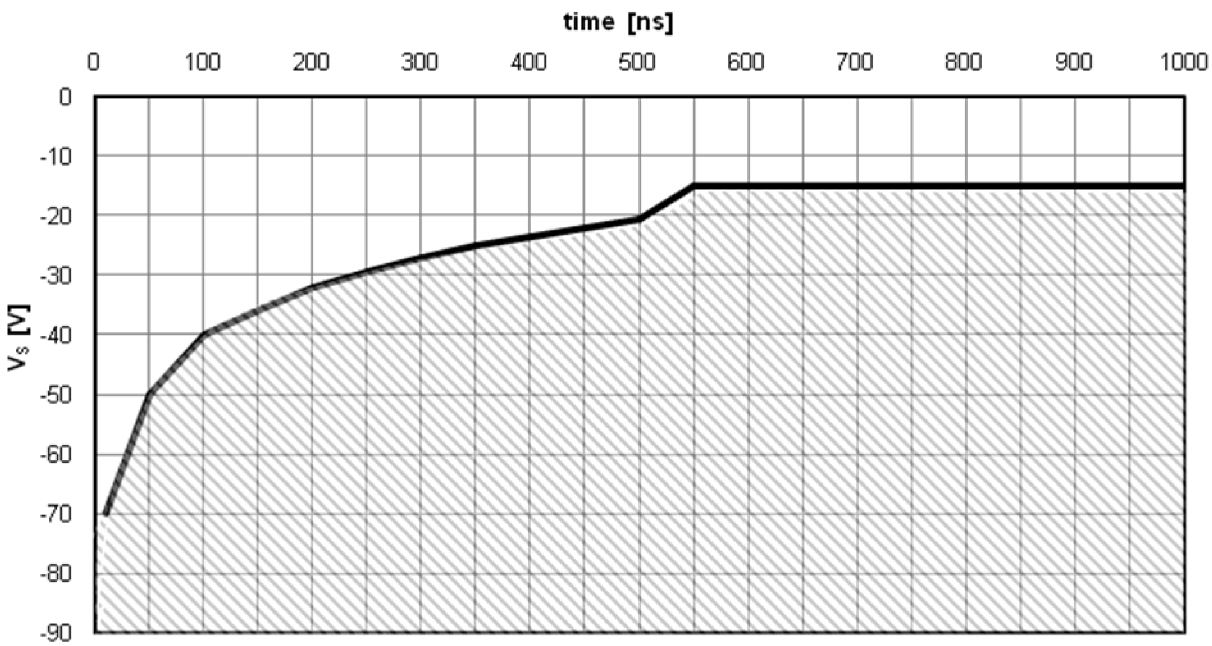


Figure 16: **Negative V_S transient SOA for IRS2607 @ VBS=15V**

Even though the IRS21867 has been shown able to handle these large negative V_S transient conditions, it is highly recommended that the circuit designer always limit the negative V_S transients as much as possible by careful PCB layout and component use.

PCB Layout Tips

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 17). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

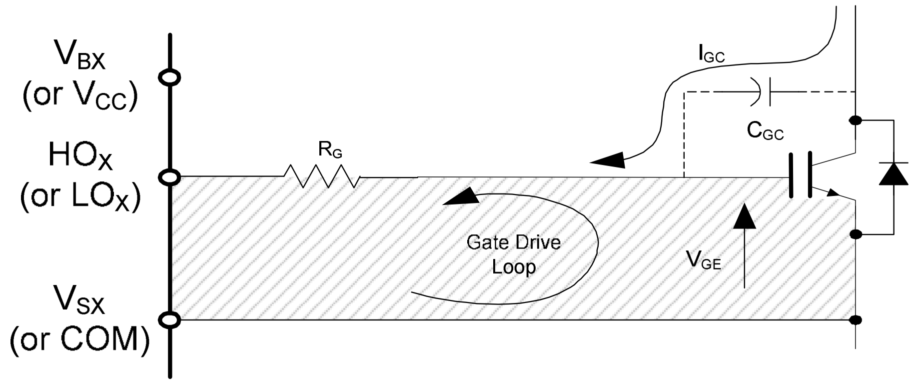


Figure 17: Antenna Loops

<u>Supply Capacitor:</u> It is recommended to place a bypass capacitor (C_{IN}) between the V_{CC} and COM pins. A ceramic 1 µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

<u>Routing and Placement:</u> Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative V_S spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the V_S pin and the switch node (see Figure 18), and in some cases using a clamping diode between COM and V_S (see Figure 19). See DT04-4 at www.irf.com for more detailed information.

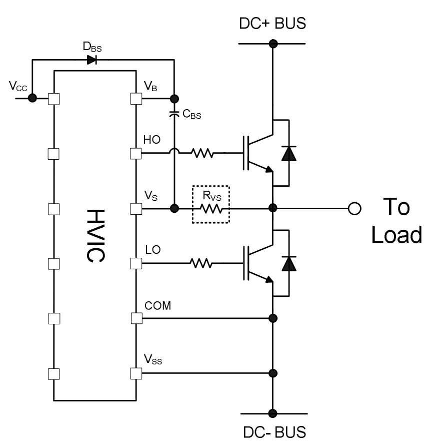


Figure 18: V_S resistor

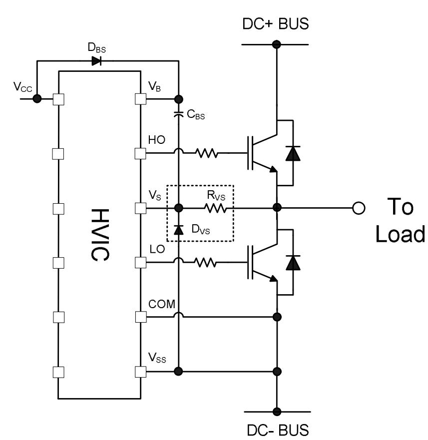


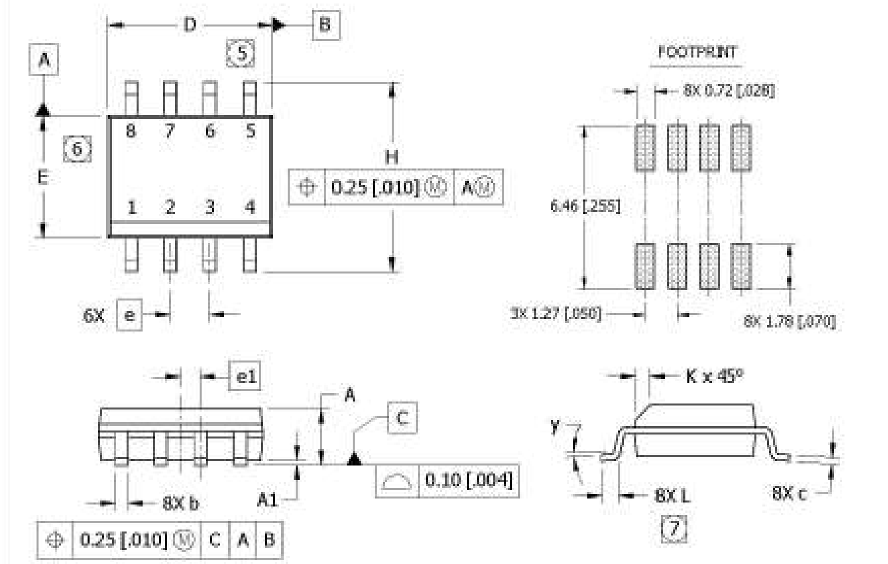
Figure 19: V_S clamping diode

Additional Documentation

Several technical documents related to the use of HVICs are available at www.irf.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

DT97-3: Managing Transients in Control IC Driven Power Stages
DT04-4: Using Monolithic High Voltage Gate Drivers
AN-978: HV Floating MOS-Gate Driver ICs

Package Details: SOIC8N



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

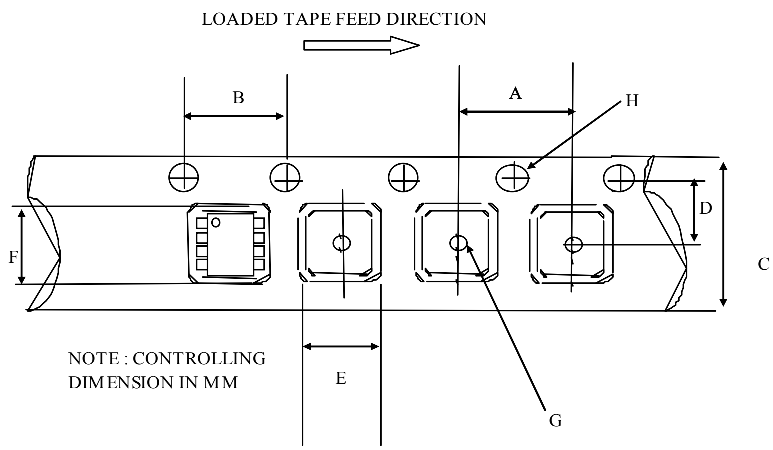
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

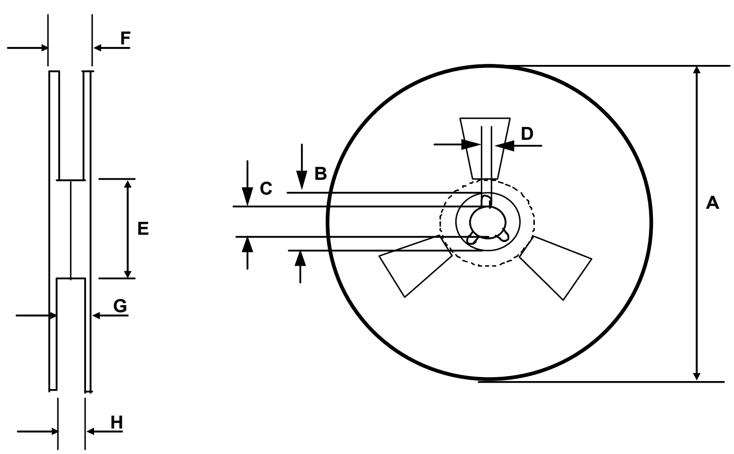
8 Lead SOIC

Tape and Reel Details: SOIC8N



CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062

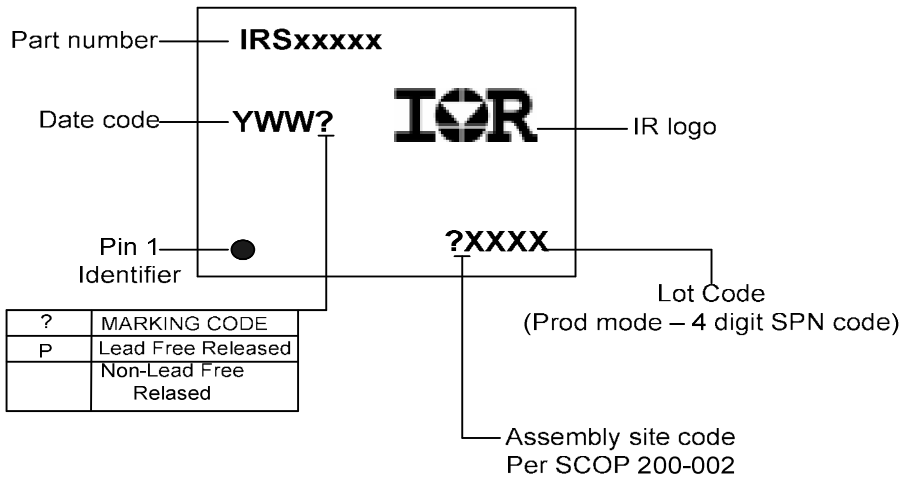


REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information

LEAD-FREE PART MARKING INFORMATION



Ordering Information

P/n	Package	Packing	Pcs
IRS21867SPbF	SOIC8	Tube	95
IRS21867STRPbF	SOIC8	Tape & Reel	2500

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

WORLD HEADQUARTERS:
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Tel: (310) 252-7105

Revision History

Date	Comment
5/20/2010	Initial Draft
6/10/2010	Changed ABS MAX to 25V, Updated Iin+ to 250uA(Typ) to reflect 20kohm pull-down, Removed Min spec (2A) from Io+/Io-, Updated Block Diagram based on IRS2188 D/S
03/30/2011	Add recommended operation condition note
05/27/2011	Add ESD and Latch up specs
05/31/2011	Add application info and ordering info