FQP15N60/FQPF15N60

## 600V 15A Super Junction MSFET

General Description

The FQP15N60& FQPF15N60 have been fabricated using the advanced αMOS^{TM} high voltage process that is designed to deliver high levels of performance and robustness in switching applications. By providing low R$_{DS(on)}$, Q$_g$ and E$_{OSS}$ along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

Product Summary

V$_{DS}$ @ T$_{j,max}$	700V
I$_{DM}$	63A
R$_{DS(ON),max}$	0.29Ω
Q$_{g,typ}$	16nC
E$_{oss}$ @ 400V	3.6µJ

100% UIS Tested
100% R$_g$ Tested

RoHS Compliant

Top View

TO-220   TO-220F

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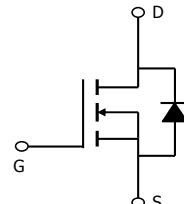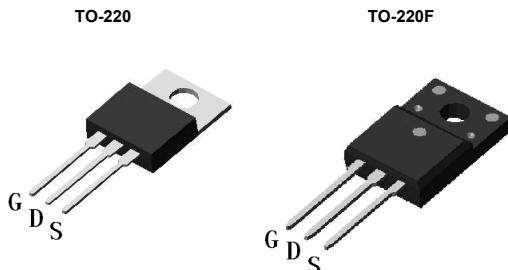
Absolute Maximum Ratings T$_A$=25°C unless otherwise noted

Parameter		Symbol	FQP15N60/FQB15N60	FQPF15N60	Units
Drain-Source Voltage		V$_{DS}$	600		V
Gate-Source Voltage		V$_{GS}$	±30		V
Continuous Drain Current	T$_C$=25°C	I$_D$	15	15*	A
	T$_C$=100°C		10	10*	
Pulsed Drain Current ^{C}		I$_{DM}$	63		
Avalanche Current ^{C}		I$_{AR}$	2.4		A
Repetitive avalanche energy ^{C}		E$_{AR}$	86		mJ
Single pulsed avalanche energy ^{G}		E$_{AS}$	173		mJ
Power Dissipation ^{B}	T$_C$=25°C	P$_D$	208	27.8	W
	Derate above 25°C		1.67	0.22	W/ ^{o}C
MOSFET dv/dt ruggedness		dv/dt	100		V/ns
Peak diode recovery dv/dt ^{H}			20		
Junction and Storage Temperature Range		T$_J$, T$_{STG}$	-55 to 150		°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds ^{J}		T$_L$	300		°C

Thermal Characteristics

Parameter	Symbol	FQP15N60/FQB15N60	FQPF15N60	Units
Maximum Junction-to-Ambient ^{A,D}	R$_{θJA}$	65	65	°C/W
Maximum Case-to-sink ^{A}	R$_{θCS}$	0.5	--	°C/W
Maximum Junction-to-Case	R$_{θJC}$	0.6	4.5	°C/W

* Drain current limited by maximum junction temperature.

Electrical Characteristics (T$_J$=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV$_{DSS}$	Drain-Source Breakdown Voltage	I$_D$=250µA, V$_{GS}$=0V, T$_J$=25°C	600	-	-	V
		I$_D$=250µA, V$_{GS}$=0V, T$_J$=150°C	650	700	-	
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$=600V, V$_{GS}$=0V	-	-	1	µA
		V$_{DS}$=480V, T$_J$=150°C	-	10	-	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$=±30V	-	-	±100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=5V, I$_D$=250µA	2.5	3.2	3.8	V
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$=10V, I$_D$=7.5A, T$_J$=25°C	-	0.254	0.29	Ω
		V$_{GS}$=10V, I$_D$=7.5A, T$_J$=150°C	-	0.68	0.78	Ω
V$_{SD}$	Diode Forward Voltage	I$_S$=7.5A, V$_{GS}$=0V, T$_J$=25°C	-	0.83	-	V
I$_S$	Maximum Body-Diode Continuous Current		-	-	15	A
I$_{SM}$	Maximum Body-Diode Pulsed Current[C]		-	-	63	A
DYNAMIC PARAMETERS						
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$=100V, f=1MHz	-	717	-	pF
C$_{oss}$	Output Capacitance		-	58	-	pF
C$_{o(er)}$	Effective output capacitance, energy related [H]	V$_{GS}$=0V, V$_{DS}$=0 to 480V, f=1MHz	-	41.2	-	pF
C$_{o(tr)}$	Effective output capacitance, time related [I]		-	125.2	-	pF
C$_{rss}$	Reverse Transfer Capacitance	V$_{GS}$=0V, V$_{DS}$=100V, f=1MHz	-	1.3	-	pF
R$_g$	Gate resistance	V$_{GS}$=0V, V$_{DS}$=0V, f=1MHz	-	13.4	-	Ω
SWITCHING PARAMETERS						
Q$_g$	Total Gate Charge	V$_{GS}$=10V, V$_{DS}$=480V, I$_D$=7.5A	-	15.6	-	nC
Q$_{gs}$	Gate Source Charge		-	3.5	-	nC
Q$_{gd}$	Gate Drain Charge		-	6.0	-	nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$=10V, V$_{DS}$=400V, I$_D$=7.5A, R$_G$=25Ω	-	24.5	-	ns
t$_r$	Turn-On Rise Time		-	22	-	ns
t$_{D(off)}$	Turn-Off DelayTime		-	84	-	ns
t$_f$	Turn-Off Fall Time		-	24	-	ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$=7.5A, dI/dt=100A/µs, V$_{DS}$=400V	-	282	-	ns
I$_{rm}$	Peak Reverse Recovery Current	I$_F$=7.5A, dI/dt=100A/µs, V$_{DS}$=400V	-	26	-	A
Q$_{rr}$	Body Diode Reverse Recovery Charge	I$_F$=7.5A, dI/dt=100A/µs, V$_{DS}$=400V	-	4.5	-	µC

A. The value of R$_{θJA}$ is measured with the device in a still air environment with T$_A$=25°C.

B. The power dissipation P$_D$ is based on T$_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T$_{J(MAX)}$=150°C, Ratings are based on low frequency and duty cycles to keep initial T$_J$ =25°C.

D. The R$_{θJA}$ is the sum of the thermal impedance from junction to case R$_{θJC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T$_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

G. L=60mH, I$_{AS}$=2.4A, V$_{DD}$=150V, Starting T$_J$=25°C

H. C$_{o(er)}$ is a fixed capacitance that gives the same stored energy as C$_{oss}$ while V$_{DS}$ is rising from 0 to 80% V$_{(BR)DSS}$.

I. C$_{o(tr)}$ is a fixed capacitance that gives the same charging time as C$_{oss}$ while V$_{DS}$ is rising from 0 to 80% V$_{(BR)DSS}$.

J. Wavesoldering only allowed at leads.

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**
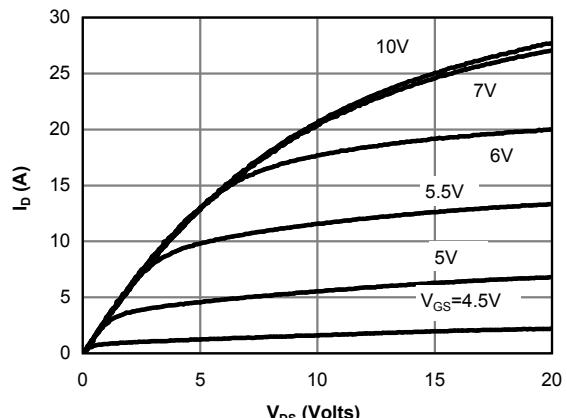
Figure 1: On-Region Characteristics@25°C
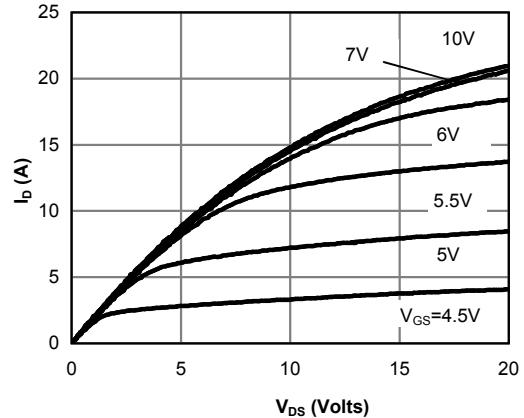
Figure 2: On-Region Characteristics@125°C
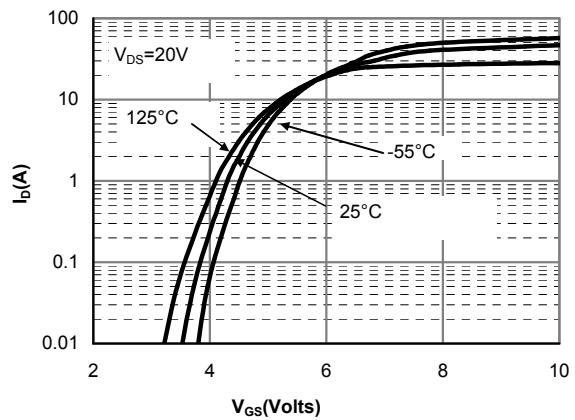
Figure 3: Transfer Characteristics
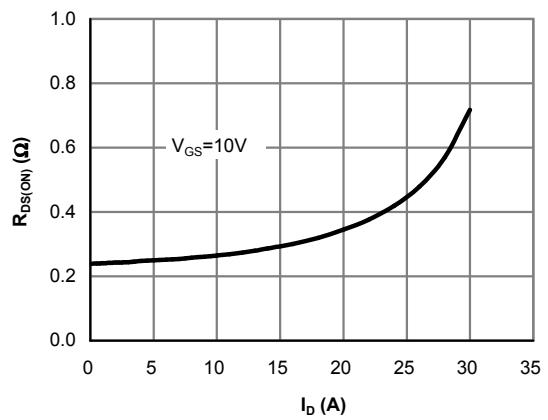
Figure 4: On-Resistance vs. Drain Current and Gate Voltage
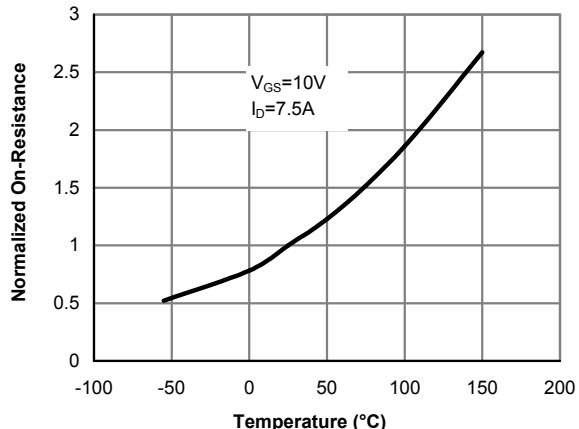
Figure 5: On-Resistance vs. Junction Temperature
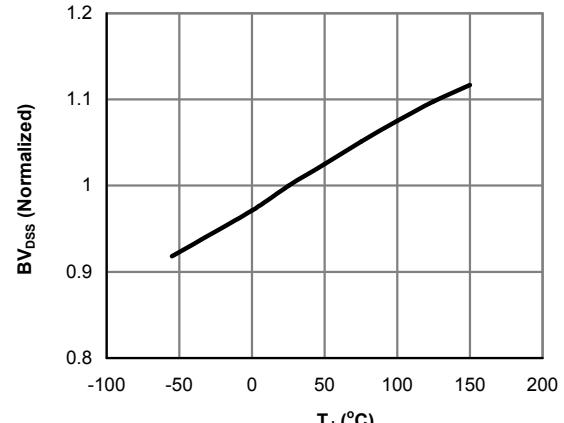
Figure 6: Break Down vs. Junction Temperature

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**
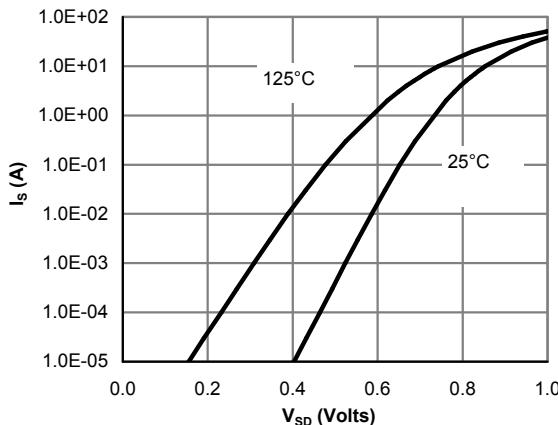
**Figure 7: Body-Diode Characteristics (Note E)**
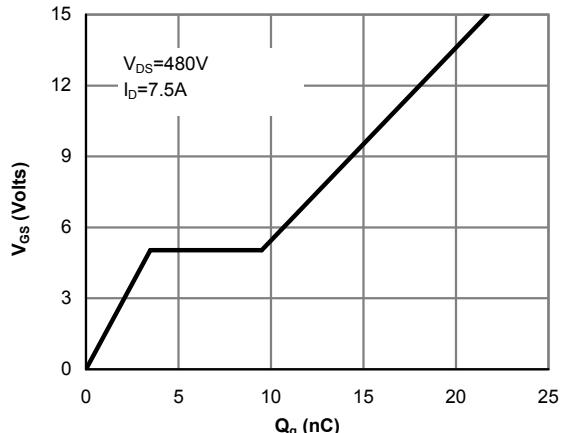
Figure 8: Gate-Charge Characteristics
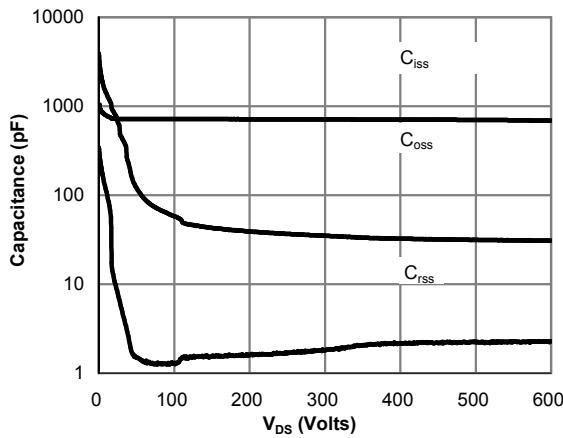
Figure 9: Capacitance Characteristics
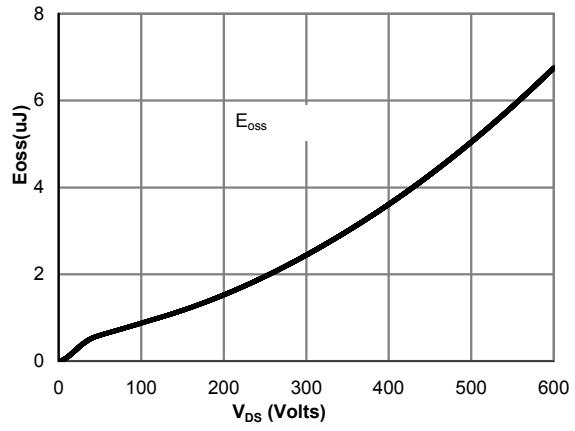
Figure 10: Coss stroed Energy
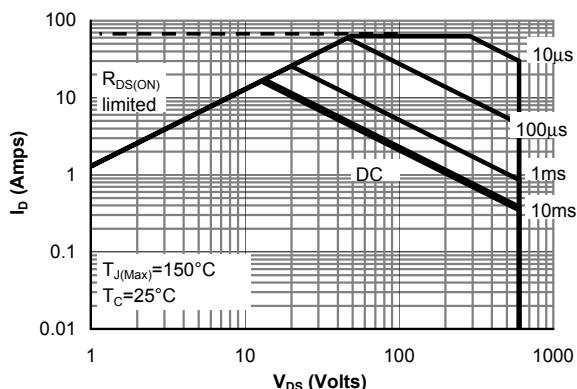
Figure 11: Maximum Forward Biased Safe Operating Area for AOT(B)15S60 (Note F)
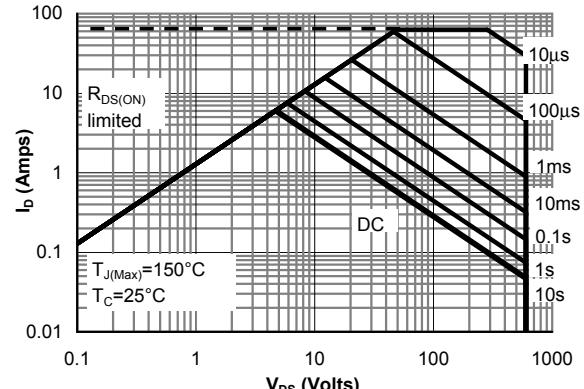
Figure 12: Maximum Forward Biased Safe Operating Area for AOTF15S60L(Note F)

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**
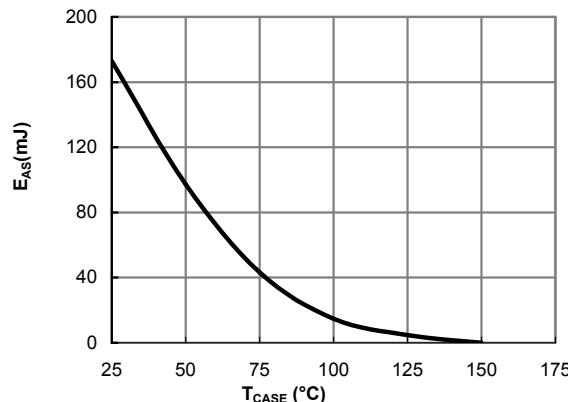
Figure 13: Avalanche energy
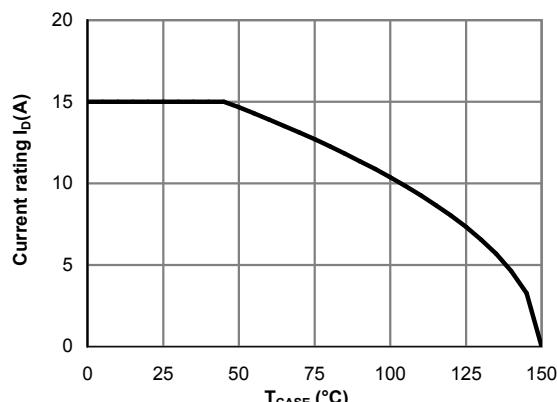

Figure 14: Current De-rating (Note B)
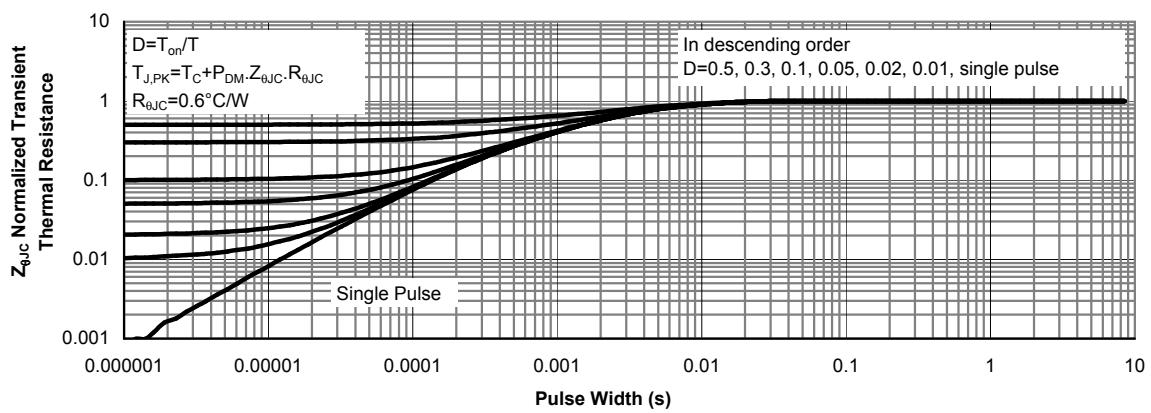
**Figure 15: Normalized Maximum Transient Thermal Impedance for AOT(B)15S60 (Note F)**

$D = T_{on}/T$
$T_{J,PK} = T_C + P_{DM} \cdot Z_{\theta JC} \cdot R_{\theta JC}$
$R_{\theta JC} = 0.6°C/W$

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

Single Pulse
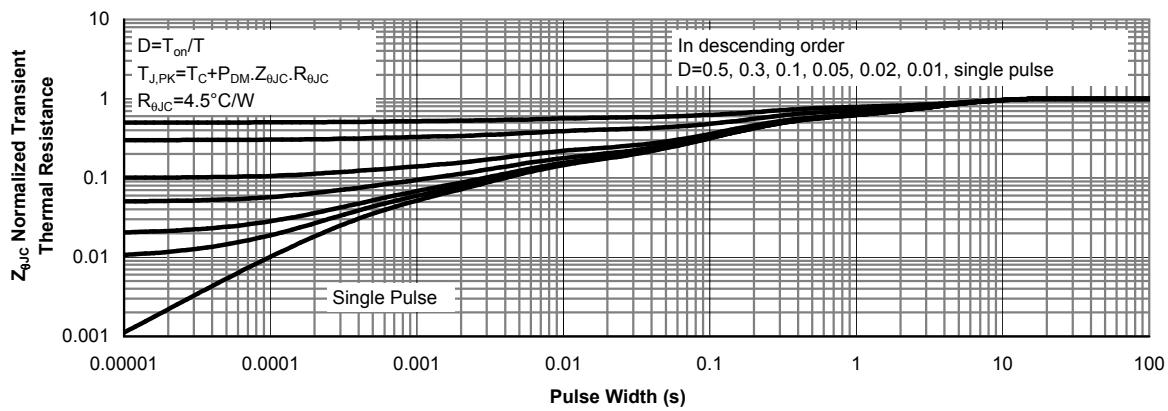
Figure 16: Normalized Maximum Transient Thermal Impedance for AOTF15S60L (Note F)

$D = T_{on}/T$
$T_{J,PK} = T_C + P_{DM} \cdot Z_{\theta JC} \cdot R_{\theta JC}$
$R_{\theta JC} = 4.5°C/W$

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

Single Pulse

Gate Charge Test Circuit & Waveform
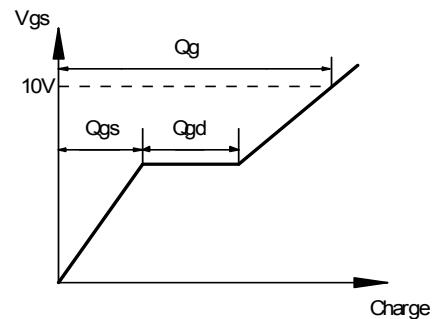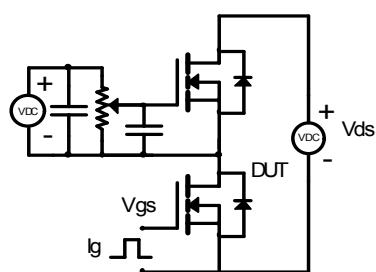
Resistive Switching Test Circuit & Waveforms
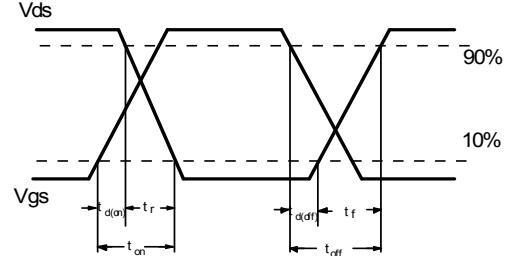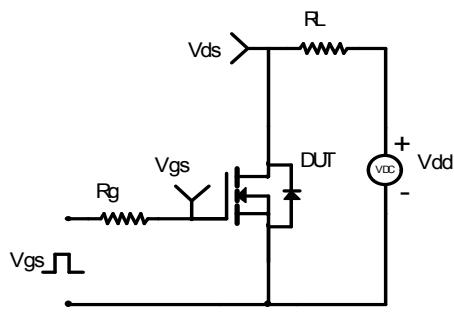
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

$$E_{AR} = 1/2\, L I_{AR}^2$$
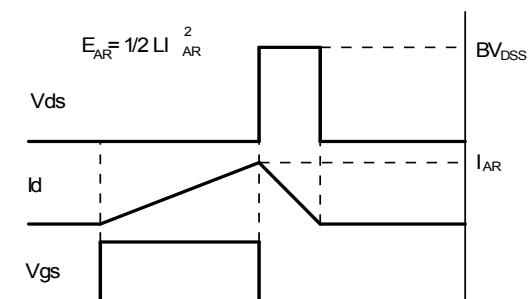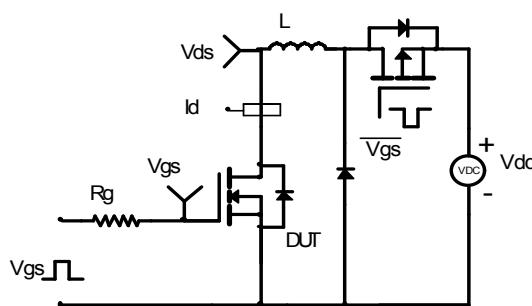
Diode Recovery Test Circuit & Waveforms

$$Q_{rr} = -\int I dt$$